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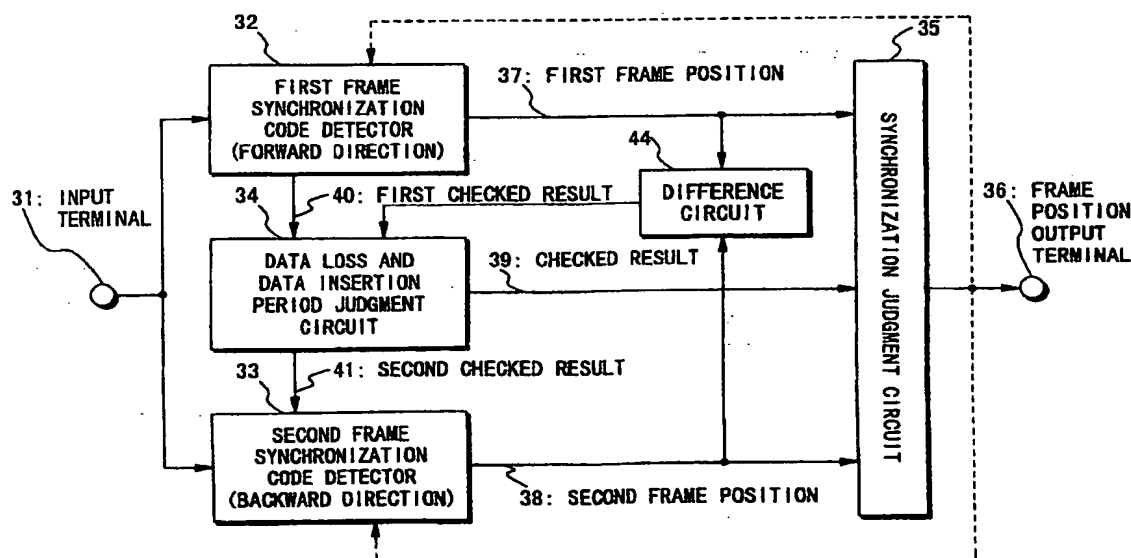
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(54) FRAME SYNCHRONIZING CIRCUIT

(57) A frame synchronizing circuit which does not cause out-of-synchronism resulting from data disappearance/insertion while suppressing the mis-synchronization/asynchronization caused by representative code errors of the conventional data transmission system. The frame synchronizing circuit is provided with a frame synchronizing code detecting circuit (32) which detects a frame synchronizing code from a received

data sequence, and outputs a frame position and collation results by collating the detected frame synchronizing code with a correct frame synchronizing code, and a data disappearance and data-insertion section judging circuit (54) which judges whether or not data disappearance or data is inserted in the received data sequence based on the collation results.

FIG. 8



Description

Field of the Invention

[0001] The present invention relates to a frame synchronization circuit suitable to transmit data sequence which have a frame composition in the environment where a code error, especially a data loss or data insertion in units of cells or packets, is prone to generate.

Background of the Invention

[Method for adding a frame synchronization code]

[0002] Conventionally, in a data transmission system in which an information data to be transmitted (transmission information data) is transmitted in frame unit, a method for adding a unique word such as M sequence to each frame as a frame synchronization code has been widely used on its transmitting side. The position to which the unique word is added is not particularly defined in this method, but in general, the unique word is set to the head of a frame to simplify the composition, as shown in FIG. 1A. The unique word in the received data sequence is detected on the reception side, so that the frame position is identified to detect each frame and a transmission information data is reproduced from the each frame detected.

[0003] However, there is a disadvantage that a phenomenon (out of detection) which can not detect the unique word is often occurred due to burst code error or the like, if the method is applied to the data transmission in a transmission channel where the code error is prone to generate. As such, there is proposed a technique in which the resistance to the burst code error is improved by positioning unique words scatteredly within a frame.

[0004] An example of such frame composition concerning this technique is shown in FIGs. 1B and 1C. These figures show arrangements of identical unique words. That is, FIG. 1C displays an information data for every block of predetermined length ($M + 1$ bits) and FIG. 1B expands the information data for every one bit. In FIG. 1C, unique words are constituted of the most significant bit (bits S1 to SN) of each block, and the signal shown in FIG. 1B can be obtained by expanding the unique words to a serial data from high order bit sequentially.

[0005] In the example shown in FIG. 1B, the unique words S_j ($j = 1$ to N) are assigned one bit to each uniform interval (M bits) in a transmission information data sequence. However, the intervals assigned may be non-uniform and also plural bits may be assigned. Incidentally, M and N are natural numbers.

[0006] Most of the unique words would survive even if a burst code error generates in a transmission channel by positioning unique words scatteredly in this way, so that the phenomenon which can not detect any of the unique words is avoided by permitting the disagree-

ments of the number of constant bits at the time of detection, allowing detection of the unique words with high probability. Incidentally, if the number of disagreement bits permitted is too large compared with the unique word length, there may be occurred a phenomenon (false detection) in which a part of information data is detected by mistake as a unique word, so that the number of disagreement bits and the unique word length must be set such that the probability of occurring the false detection can be restrained sufficiently low.

[0007] Moreover, if a frame length is variable, to achieve higher frame synchronization property, a frame length information can also be used in addition to the unique word as a frame synchronization code, as shown in FIG. 1D. An appearance position of the following frame synchronization code can be known on the reception side by using the frame length information, so that the probability of occurring the out of detection or false detection of the frame synchronization code can be reduced compared with the case in which only the unique word is used.

[Composition and operation of conventional frame synchronization circuit]

[0008] Next, there are described the composition and operation of a conventional frame synchronization circuit.

Incidentally, as a method for adding unique words to a frame, a head arrangement or scattered positioning described above can be considered, and there is no influence in the following explanation even if either is adopted.

A. In the case of a fixed length frame

[0009] FIG. 2 shows a composition of a conventional frame synchronization circuit (Example 1). The frame synchronization circuit shown in FIG. 2 is premised to be applied to a transmission system of a fixed length frame. As shown in FIG. 2, a received data sequence input from an input terminal 11 is sent to a unique word detector 12. In the unique word detector 12, an input buffer 15 buffers the received data sequence sent from the input terminal 11, cuts out data equivalent to the unique word length at every predetermined timing to supply the data to a comparator 16, and then shifts a cut out position of the data by one bit at every same timing.

[0010] The comparator 16 compares the data supplied from the input buffer 15 and the unique word given from a unique word generator 17, and supplies "1" when the data is in accordance with the unique word or "0" when both are in disagreement to a synchronization judgment circuit 13 as a comparison result. In this case, in order to prevent the out of detection based on code error occurred when comparison operation is performed in the comparator 16, the disagreement of the number of constant bits may be permitted to provide "agree-

ment".

[0011] Next, the operation of the synchronization judgment circuit 13 will be described. FIG. 3 is a state transition chart of the synchronization judgment circuit 13. The synchronization judgment circuit 13 is, at first, in an out of synchronization state S1 in which frame synchronization is not established at all. The synchronization judgment circuit 13 in the out of synchronization state S1 transfers its own state to a backward 1 state S2 as "detection", when "1" is supplied from the comparator 16, and holds its own state in the out of synchronization state S1 as "out of detection", when "0" is supplied.

[0012] The synchronization judgment circuit 13 transferred to the backward 1 state S1 skips the received data sequence by the fixed frame length to wait for the output of the comparator 16. When the comparison result from the comparator 16 is "1", the synchronization judgment circuit 13 transfers its own state to a next backward 2 state S3 as "detection", and when it is "0", returns back to the out of synchronization state S1 as "out of detection". The processing similar to that described above is also performed in states after the backward 2, and the state of the synchronization judgment circuit 13 returns immediately back to the out of synchronization state S1 in the case of out of detection, and advances toward a synchronization establishment state S5 when "detection" continues for total of N+1 times.

[0013] Here, the states from the backward 1 to the backward N are set to reduce occurrence frequency of false synchronization, and generally, such setting is called as "backward protection". When the backward protection is not set up, if the part which agrees with a unique word accidentally exists somewhere in the part other than the unique word in the received data sequence, a false detection which detects the unique word by mistake may occur, resulting in frequent false synchronization. However, the synchronization judgment circuit 13 illustrated in the present invention is provided with a backward protection and also repeats agreement judgment for N+1 times to reduce the occurrence frequency of the false synchronization due to false detection.

[0014] Moreover, the synchronization judgment circuit 13, even when in the synchronization establishment state S5, skips the received data sequence only by the fixed frame length to wait an output from the comparator 16. When "1" is supplied from the comparator 16, the synchronization judgment circuit 13 retains its own state in the synchronization establishment state S5 as "detection", and when "0" is supplied, transfers its own state to a forward 1 state S6 as "out of detection". The processes in the states from the forward 1 to a forward M are contrary to those in the states from the backward 1 to the backward N described above, and in the case of "detection", the process returns immediately to the synchronization establishment state S5, and when "out of detection" continues for total of M+1 times, the process

returns back to the out of synchronization state S1. Furthermore, the states from the forward 1 to the forward M are provided in order to avoid frequent occurrence of "synchronous error", and such setting is generally called as "forward protection". When the forward protection is not provided, the synchronization may be come out immediately when the out of detection due to code error occurs. However, the synchronization judgment circuit 13 illustrated in the example is provided with the forward protection and repeats the agreement judgment for M+1 times to reduce the occurrence frequency of the "synchronous error".

B. In the case of variable length frame

B-1. When synchronization judgment is achieved in accordance with the state transfer shown in FIG. 3

[0015] In a transmission system of variable length frame, when only unique words are used as frame synchronization codes, the synchronization can also be established using a circuit of the similar composition as Example 1 shown in FIG. 2, except the function and operation of the synchronization judgment circuit 13. However, in a data transmission system using the variable length frame, the appearance position of the following frame synchronization code can not be forecasted in advance on the reception side, so that the synchronization can not be established stably by performing the state transfer shown in FIG. 3, and the unique words have to be detected by shifting a received data sequence by one bit sequentially for all frames. For this reason, the trial frequency of the unique word detection will be increased, resulting in higher occurrence frequency of false detection. Therefore, in the example, the composition and operation of the frame synchronization circuit will be described in which not only the unique word but also the frame length information are used as the frame synchronization code.

[0016] FIG. 4 shows a composition of a conventional frame synchronization circuit (Example 2) using the unique word and frame length information as the frame synchronization code. In FIG. 4, the common parts to each part of FIG. 2 are identified by the same reference character and their explanations will be omitted. The differences between Example 2 shown in FIG. 4 and Example 1 shown in FIG. 2 are such that the synchronization judgment circuit 13 is replaced with a synchronization circuit 13a and a frame length information detector 18 is newly provided.

[0017] The frame length information detector 18 extracts the frame length information followed by the unique word according to the received data sequence input from the input terminal 11 and a frame synchronization output supplied from the synchronization judgment circuit 13a to the output terminal 14, and supplies an output data to the synchronization judgment circuit 13a after decoding is performed. Incidentally, when an

error is contained in the frame length information, the synchronization judgment for the received data sequence, as will be described hereinafter, may be affected, so that the error correction and detection process (coding and decoding) is often provided to the frame length information in order to improve the reliability of the frame length information.

[0018] The synchronization judgment circuit 13a, presumes a position of the following frame synchronization code using the frame length information supplied from the frame length information detector 18 when detecting the frame synchronization code, and skips over the received data sequence to the presumed position concerned to wait for the output of the comparator 16. The operation except having described above is as similar to that of Example 1, therefore, the synchronization judgment according to the state transfer shown in FIG. 3 can be performed as with the fixed length frame, allowing the establishment of the stable synchronization.

B-2. When synchronization judgment is achieved without following the state transfer shown in FIG. 3

[0019] Next, a conventional frame synchronization circuit (Example 3) will be explained in which the synchronization judgment is achieved without following the state transfer shown in FIG. 3. In the data transmission system using the variable length frame shown in FIG. 3, the unique word and frame length information are used as the frame synchronization codes, and the error correction and detection processes are premised to be applied to the frame length information. When the frame length information without error is detected in a position followed by the unique word, it is judged that a correct frame synchronization code has been detected. According to Example 3, the occurrence frequency of false detection can be more reduced than if only the unique word is used as the frame synchronization code, so that the frame synchronization position can be judged with high reliability without adopting the state transfer shown in FIG. 3.

[0020] As will be apparent from a manner described above, the conventional frame synchronization circuit for a fixed and variable length frames operate effectively in either case for a typical code error, such as a random error and burst error, in a conventional transmission system.

[0021] However, a transmission system in which a new code error different type from that described above may be generated has appeared in recent years. For example, in an ATM (Asynchronous Transfer Mode) transmission, a data loss (cell loss) in packet units of 48 bytes to 53 bytes may occur, when a traffic is too large as compared with transmission channel capacity. Moreover, on an Internet, there has occurred the data loss with a packet unit longer than that described above. Furthermore, in a so-called multimedia transmission, coded data corresponding to plural display media are multi-

plexed, so that when a code error occurs in an information indicating a multiplexed pattern, separating is performed using a wrong pattern, causing data loss or data insertion in packet units.

[0022] When a conventional frame synchronization circuit is applied to a data transmission system in which a code error of this type may occur, there appears a problem that the synchronization property is substantially degraded.

[0023] Here, there is shown an example of data loss/insertion in FIGs. 5A to 5D. As shown in FIGs. 5A to 5D, when a data loss (packet loss) occurs in a received data sequence FIG. 5A, the length of the frame in which data loss has occurred is made shorter than an original frame length 5B. And, when data insertion (packet insertion) has occurred in the received data sequence 5C, the length of the frame in which data insertion has occurred is made longer than the original frame length 5D.

[0024] When the data loss/insertion is generated while the frame synchronization circuit (Example 1 and 2) adopted the state transfer of FIG. 3 is in the synchronization establishment state, false frame synchronization positions are output continuously for the number of the frames which is "1" larger than the number of stages (M) of the forward protection, causing the continuous synchronous error. In addition, in order to recover the synchronization, the frame synchronization codes of the number, which adds 1 to the number of stages (N) of the backward protection must be detected continuously. That is, there is a disadvantage that the period of synchronous error is long.

[0025] Moreover, in order to reduce the time (number of frames) of the continuous synchronous error described above, a countermeasure of reducing the number of stages of the forward and backward protection can be considered. However, when this countermeasure is tried, a drawback will come out which can not maintain the strength to the typical code error, such as a random error or burst error, in a conventional transmission system, and also a countermeasure other than that having such a drawback has not been known.

[0026] On the one hand, in the frame synchronization circuit (Example 3) which does not use the state transfer of FIG. 3 in a data transmission system using variable length frames, although the continuous synchronous error described above does not occur, frames which are shorter or longer than those expressed with the frame length information included in the frame synchronization code are received, so that the following frame synchronization position can not be detected correctly, thereby the synchronization codes can not be detected not only in frames in which the data loss/insertion has occurred but also in frames followed by the frames, resulting in synchronous error of at least total of two frames.

[0027] Furthermore, even when the following frame synchronization code can be detected correctly, only an alarm can be issued to indicate errors in the frame

length of frames where the data loss/insertion has occurred, so that data with false length which includes discontinuity in the middle of a frame will be output. Therefore, there is a problem in which a decoder (corresponding to display media) followed by the frame synchronization circuit can not decode data from the frame synchronization circuit correctly. In addition, a decoder applied to a transmission channel where code error may exist is often provided with error protection functions, such as error correction function or bit interleave function, but when discontinuity exists in the middle of data supplied from the frame synchronization circuit or the length of a whole data is wrong, the above-mentioned function does not work at all.

Disclosure of the Invention

[0028] The present invention has been made in an attempt to solve the above-described problems, and therefore, has a first object to provide a frame synchronization circuit which can prevent the occurrence of synchronous error due to data loss/insertion while restraining the false synchronization/out of synchronization according to the typical code error, such as random error and burst error, in a conventional transmission system.

[0029] It is a second object to provide a frame synchronization circuit which can reduce the adverse effect affecting a following circuit by correcting a received data sequence.

[0030] To solve the above described problem, in the present invention,

a frame synchronization circuit used on a reception side in a data transmission system adopting a frame composition positioning a frame synchronization code scatteredly in a frame is characterized by comprising:

a frame synchronization code detector detecting a frame synchronization code from a received data sequence to output a frame position and outputting a check result by checking a frame synchronization code detected and a correct frame synchronization code; and

a data loss and data insertion period judgment circuit presuming whether a data loss or data insertion has occurred in said received data sequence according to said check result.

Brief Description of the Drawings

[0031]

FIGs. 1A to 1D are drawings for explaining how to add the frame synchronization code.

FIG. 2 is a block diagram showing a composition of a conventional frame synchronization circuit (Example 1).

FIG. 3 is a state transfer chart of a synchronization judgment circuit 13 in Example 1.

FIG. 4 is a block diagram showing a composition of a conventional frame synchronization circuit (Example 2).

FIGs. 5A to 5D are drawings showing one example of a received data sequence in which data loss and data insertion have occurred.

FIG. 6 is a schematic view showing one example of the received data sequence in this embodiment.

FIGs. 7A to 7H are drawings extracting and showing only a portion of the frame synchronization code from the received data sequence shown in FIG. 6.

FIG. 8 is a block diagram showing a composition (composition 1) of a frame synchronization circuit according to an embodiment of the present invention.

FIG. 9 is a block diagram showing a composition (composition 2) of a modification of a frame synchronization circuit according to an embodiment of the present invention.

FIGs. 10A to 10M are drawings extracting and showing only a portion of the frame synchronization code from the received data sequence illustrated in FIG. 6.

FIGs. 11A to 11M are drawings extracting and showing only a portion of the frame synchronization code from the received data sequence illustrated in FIG. 6.

FIG. 12 is a block diagram showing an example of internal composition (example of internal composition 1) of each frame synchronization code detector.

FIGs. 13A to 13K are drawings extracting and showing only a portion of the frame synchronization code from the received data sequence illustrated in FIG. 6.

FIGs. 14A to 14P are drawings extracting and showing only a portion of the frame synchronization code from the received data sequence illustrated in FIG. 6.

FIGs. 15A to 15P are drawings extracting and showing only a portion of the frame synchronization code from the received data sequence illustrated in FIG. 6.

FIG. 16A to 16P are drawings extracting and showing only a portion of the frame synchronization code from the received data sequence illustrated in FIG. 6.

FIG. 17 is a block diagram showing a composition when a frame synchronization code detector according to an embodiment of the present invention is applied to a variable length frame.

FIG. 18 is a block diagram showing a composition when a frame synchronization code detector according to an embodiment of the present invention is applied to a variable length frame.

FIG. 19 is a block diagram showing the composition

of the frame synchronization circuit according to another embodiment.

FIGs. 20A to 20G are drawings explaining the operation of the embodiment in FIG. 19 when a code error has occurred.

FIGs. 21A to 21G are drawings explaining the operation of the embodiment in FIG. 19 when data loss has occurred.

The Best Form for Executing the Invention

(Principle of the Embodiment)

[0032] The fundamental idea of this embodiment has resulted from the skillful use of the following facts and characteristics.

(1) When the data loss/insertion in packet units has occurred, a portion of a frame synchronization code along with the information data will be lost, by using the frame composition positioning the frame synchronization code scatteredly in a frame.

(2) When observing a frame synchronization code from both directions, in the forward direction (positive direction on time axis) and backward direction (opposite direction on time axis), in a received data sequence, there is a characteristic that when only a usual code error has occurred, the code error will be found in the same position, while a data loss/insertion has occurred in packet units, the code error will be found in the different position.

(3) In addition, the position and the length of the lost frame synchronization code can be presumed from the position and the length where the disagreement has occurred. The position and the length of the lost information data can also be presumed using the presumed result of the position and the length of the lost frame synchronization code, so that the information data with correct length can be reproduced by inserting a dummy data into the period judged to be a data loss period and deleting the data concerned from the period judged to be the data insertion period.

(4) As a result, the data loss in packet units can be transformed into a usual burst error, and the data insertion can be removed completely in an ideal case.

[0033] In a preferred embodiment according to the above-mentioned facts and characteristics, a frame synchronization circuit used on the reception side of a data transmission system adopting a frame composition positioning a frame synchronization code scatteredly in a frame is characterized by comprising:

a first frame synchronization code detector detecting a frame synchronization code by checking a received data sequence with a correct frame syn-

chronization code in the forward direction on time axis to output the detected position as a first frame position and also outputting the checked result as a first checked result;

a second frame synchronization code detector detecting a frame synchronization code by checking said received data sequence with the correct frame synchronization code in the opposite direction on time axis to output a detected position as a second frame position and also outputting the checked result as a second checked result;

a difference circuit detecting a length from said first frame position to a second frame position immediately after the first frame position;

a frame length information output means outputting a frame length information;

a data loss and data insertion period judgment circuit presuming a data loss period or data insertion period included in said received data sequence according to said frame length information, a length output from said difference circuit, said first checked result, and said second checked result; and

a synchronization judgment circuit determining and outputting a frame synchronization position based on said first frame position, said second frame position, and the presumed result of said data loss and data insertion period judgment circuit.

[0034] Also, in another embodiment, a dummy data insertion and deletion circuit is added to the above described composition which outputs a corrected received data sequence produced by inserting a dummy data into the presumed data loss period and deleting data from the presumed data insertion period for said received data sequence.

[0035] In yet another embodiment, said first frame synchronization code detector and said second frame synchronization code detector use frame synchronization positions output from said synchronization judgment circuit as initial values, when a data loss period or a data insertion period is presumed by said data loss and data insertion period judgment circuit.

[0036] In yet alternative embodiment, in each composition described above, said data loss and data insertion period judgment circuit, when said frame length information of a frame to be processed is different from a length output from said difference circuit, judges provisionally that a data loss has occurred in the frame,

(1) when a first start position, from which a check disagreement starts, followed by a continuous check agreement period which can be obtained from said first checked result viewed in the forward direction on time axis and is longer than a predetermined length agrees with a second start position, from which a check disagreement starts, followed by a continuous check agreement period which can

be obtained from said second checked result viewed in the backward direction on time axis and is longer than predetermined length, it is finally judged that a data loss of a number of bits corresponding to a difference between said frame length information of a frame to be processed and a length output from said difference circuit has occurred at the position,

(2) when said second start position is prior to said first start position on time axis, it is finally judged that a data loss of said number of bits has occurred in any position in the period from said second start position to said first start position,

in a case which is not applicable to either of (1) and (2), the provisional judgment is changed such that not data loss but data insertion has occurred,

(3) when a length of an period from said first start position to said second start position agrees with a length output from said difference circuit, the period is judged finally to be a data insertion period, and

(4) when the length of a period from said first start position to said second start position is shorter than the length output from said difference circuit, the period of said number of bits including the period is judged finally to be a data insertion period.

[0037] Furthermore, in another embodiment, in addition to said (1) and (2), when said first start position is prior to said second start position on time axis, it is judged finally that a data loss of said number of bits has occurred in any position in the period from said first start position to said second start position, and only when a case is not applicable to this, the final judgment of said (3) or (4) is performed for the first time.

[0038] Furthermore, in another embodiment, a frame number is used together, and in addition to said (1) and (2), when said first start position is prior to said second start position on time axis and a frame number showed by said first frame position is continuous with an immediately following frame number showed by said second frame position, it is judged finally that a data loss of said number of bits has occurred in any position in the period from said first start position to said second start position, and only when a case is not applicable to this, a process is made to be advanced after said (3) for the first time, furthermore, in addition to said (3) and (4), when a length of an period from said first start position to said second start position is longer than a length output from said difference circuit, it is judged finally that a data insertion of said number of bits has occurred in any position in the period.

[0039] Furthermore, in another embodiment, a first and second threshold values are introduced, and when said frame length information of a frame to be processed is different from a length output from said difference circuit and the difference of the both is shorter than a predetermined first threshold value, said data loss and data insertion period judgment circuit judges

provisionally that a data loss has occurred in the frame, and in addition to said (1) and (2), when said first start position is prior to said second start position on time axis, it is judged finally that a data loss of said number of bits has occurred in any position in the period from said first start position to said second start position, when said frame length information of said frame is different from a length output from said difference circuit and also the length output from said difference circuit is shorter than a predetermined second threshold value, it is judged provisionally that a data insertion has occurred in the frame, and in addition to said (3) and (4), when a length of an period from said first start position to said second start position is longer than a length output from said difference circuit, it is judged finally that a data insertion of said number of bits has occurred in any position in the period.

[0040] According to each embodiment described above, even if a data loss and data insertion in packet units may occur, a frame synchronous error does not come out and also the position and length of the data loss and data insertion can be presumed correctly. Moreover, an information data with correct length can be reproduced by inserting a dummy data into the period judged to be a data loss period and by deleting the data of the period concerned from the period judged to be a data insertion period. As a result, a data loss in packet units can be transformed into a burst error, and even if a data insertion may occur, the effect resulted from this can be removed completely in an ideal case. Also, when a frame length information is included in a frame synchronization code or a unique word is set properly, this embodiment can be applied not only to a fixed length frame but also to a variable length frame. Of course, there is especially no limitation for the position and length of data loss/insertion which can be presumed and compensated.

(The First Embodiment)

[0041] The present invention will hereinbelow be described in further detail with reference to the accompanying drawings.

[0042] The present embodiment is based on the composition corresponding to a frame synchronization circuit concerned with claim 1 and the function corresponding to a frame synchronization circuit concerned with claim 4, so that thereafter the explanation will be advanced based on this basic composition and function. However, the explanation will be added to embodiments with distinctive composition of frame synchronization circuits concerned with other claims to clarify the relations to each claim.

A. Composition of Frame Synchronization Circuit

A-1. Composition shown in FIG. 8

[0043] FIG. 8 is a block diagram showing a composition (Composition 1) of a frame synchronization circuit according to an embodiment of the present invention. In this drawing, 31 is an input terminal into which a received data sequence is input, 32 is a first synchronization code detector which checks the received data sequence input from the input terminal 31 and a unique word produced inside of the frame synchronization circuit on time axis in the forward direction and outputs a first checked result 40 and a first frame position 37 which is a synchronization position candidate based on the checked result concerned. And, symbol 33 designates a second synchronization code detector which checks the received data sequence input from the input terminal 31 and a unique word produced inside of the frame synchronization circuit on time axis in the backward direction and outputs a second checked result 41 and a second frame position 38 which is a synchronization position candidate based on the checked result concerned.

Incidentally, checking on time axis in the forward direction is referred to as a processing which views the received data sequence in the order of reception and also views the reference unique word in the order corresponding to this sequence to compare for every corresponding bit. And, checking on time axis in the backward direction is referred to as a processing which views the received data sequence in the opposite order of reception and also views the reference unique word in the order corresponding to this opposite sequence to compare for every corresponding bit.

[0044] Symbol 44 designates a difference circuit which outputs the difference between the first frame position 37 and the second frame position 38, and 34 is a data loss and data insertion period judgment circuit which presumes a data loss/insertion period according to the first frame position 37, the second frame position 38, and the output of the difference circuit 44 and outputs the determined period as a judgment result 39. 35 is a synchronization judgment circuit which decides a frame synchronization position based on the first frame position 37, the second frame position 38, and the judgment result 39 to output it to a frame position output terminal 36. Incidentally, the presumption process of a data loss/insertion period and the decision process of the frame synchronization position, including an explanation of the operation, will be described later.

A-2. Composition shown in FIG. 9

[0045] FIG. 9 is a block diagram showing a composition (Composition 2) of a modification of a frame synchronization circuit according to another embodiment of the present invention. What is greatly different between

the frame synchronization circuit shown in this Figure and the one shown in FIG. 8 is to provide a dummy data insertion and deletion circuit 42.

[0046] The dummy data insertion and deletion circuit 42 corrects the received data sequence input from the input terminal 31 according to the output from the data loss and data insertion period judgment circuit 34 and outputs the received data sequence corrected (corrected received data sequence) through a corrected received data sequence output terminal 43. The concrete correction processing will be described hereinafter in an explanation of the operation. A-3. Composition where broken line parts are added to FIGs. 8 and 9

[0047] In addition, compositions (Compositions 3, 4) of modification of each frame synchronization circuit are shown in FIGs. 8 and 9 by expressing additional portions with broken lines.

[0048] Incidentally, the state transfer of FIG. 3 is adopted in either composition described above.

B. Composition of the transmission data

[0049] FIG. 6 is a schematic view showing one example of the received data sequence in this embodiment. As shown in this figure, a frame synchronization code is positioned in a frame scatteredly in the present invention. In order to avoid the explanation to be complicated in this embodiment, a frame length is defined as a fixed length, a frame synchronization code is made a unique word such as M sequence, and a method for scattered positioning is an equal interval positioning of single bits (total of N bits) at intervals of M bits. Therefore, the frame length becomes $N \times (M + 1)$ bits and the information data length becomes $N \times M$ bits. Incidentally, N and M are natural numbers.

[0050] FIG. 6 illustrates the composition of the i-th frame (i is a natural number) of a received data sequence. At the head of a frame, the first bit S1 of a frame synchronization code is arranged, subsequently M-bit information data, the second bit S2, M-bit information data, ..., the N-th bit SN, and M-bit information data are arranged. Furthermore, even when the length of the last information data block is changed in the range of 1-M bits, the frame synchronization is not affected, so that a fixed length frame of arbitrary length can actually be processed.

C. Operation when usual code error has occurred

[0051] Next, The operation according to the present embodiment will be described when a usual code error such as a random error and burst error in a conventional data transmission system.

[0052] FIGs. 7A to 7H shows only a part of frame synchronization code extracted from a received data sequence illustrated in FIG. 6. There are shown with corresponded bit position a received data sequence without code error FIG. 7A, a received data sequence in

which code errors have occurred in positions marked "x" in the figure, frame positions (first frame positions) FIG. 7C obtained when frame synchronization is performed in the forward direction on time axis to the received data sequence FIG. 7B, reference unique words FIG. 7D in the forward direction on time axis, a checked result (a first checked result) FIG. 7E between the received data sequence FIG. 7B and the reference unique words in the forward direction, frame positions (second frame positions) FIG. 7F obtained when frame synchronization is performed in the backward direction on time axis to the received data sequence FIG. 7B, reference unique words FIG. 7G in the opposite direction on time axis, and a checked result (a second checked result) FIG. 7H between the received data sequence FIG. 7B and the reference unique words in the backward direction. In the example shown in this figure, the code errors have occurred at the fourth bit S4 and sixth bit S6.

[0053] As shown in FIGs. 7A to 7H, when a usual code error has occurred, the first frame positions obtained by frame synchronization detection in the forward direction on time axis agrees with the second frame positions obtained by frame synchronization detection in the backward direction on time axis, and both designates the normal positions. Therefore, the output of the difference circuit 44 agrees with the length of the frame to be detected. However, the first frame position shows the head position of the frame to be processed (detected) and the second frame position indicates the head position of the immediately following frame of the frame concerned. Also, in the first checked result FIG. 7E and second checked result 7H, plural of "1" indicating the disagreement of check occur in the fourth bit S4 and sixth bit S6, but the both checked results are agreed completely.

[0054] As mentioned above, when two properties, that is,

- (1) the output of the difference circuit 44 agrees with the length of the frame to be detected, and
- (2) the first checked result agrees with the second checked result,

are adapted, it can interpret that usual code errors, such as a random error and burst error, may occur, so that the data loss and data insertion period judgment circuit 34 does not output any data to the synchronization judgment circuit 35. Therefore, the synchronization judgment circuit 35 outputs the first frame position or second frame position to the frame position output terminal 36 as a correct frame synchronization position (It depends on design of the circuit which of the first frame position or second frame position is output).

[0055] As described above, when a usual code error may occur, the frame synchronization circuit according to the present embodiment operates like a conventional frame synchronization circuit. Of course, the same is true of the case without code error. In addition, the sim-

ilar operation is also performed in the above described Composition 2 to 4. Incidentally, the dummy data insertion and deletion circuit 42 makes the received data sequence pass through to the corrected received data sequence output terminal 43. Moreover, in Composition 3 and 4, because the data loss and data insertion period judgment circuit 34 outputs nothing, the first frame synchronization code detector 32 and second frame synchronization code detector are not initialized.

D. Operation when only data loss occurs

[0056] Next, the operation according to the present embodiment will be described when only data loss in packet units occurs (when code error other than data loss does not occur). However, to avoid the explanation to become complicated, the data loss is defined to occur at the intervals of multiple of positioning period of the unique word. Also, in this section, after describing the process in Composition 2 previously noted, the process in Composition 1 will be described.

[0057] FIGs. 10A to 10M shows only a portion of a frame synchronization code extracted from the received data sequence illustrated in FIG. 6. There are shown in the upper part of the figure a received data sequence FIG. 10A without code error, a received data sequence FIG. 10B in which data loss has occurred in a frame, the first frame position FIG. 10C in the forward direction to the received data sequence FIG. 10B, reference unique words FIG. 10D in the forward direction on time axis, the first checked result FIG. 10E in the forward direction to the received data sequence FIG. 10B, the second frame position FIG. 10F in the backward direction to the received data sequence FIG. 10B, reference unique words FIG. 10G in the backward direction on time axis, and the second checked result FIG. 10H in the backward direction to the received data sequence FIG. 10B. In the example shown in this embodiment, as is evident from the received data sequence FIG. 10B, four bits from the fifth bit S5 to eighth bit S8 are lost due to data loss.

[0058] When such data sequence FIG. 10B is input from the input terminal 31, the received data sequence concerned is supplied to the first frame synchronization code detector 32 and the second frame synchronization code detector 33.

[0059] Here, an inner composition example (Inner composition example 1) of each frame synchronization code detector is shown in FIG. 12. The inner composition example 1 shown in this figure is composed of a reception data input terminal 21, a unique word detector 22 which compares the received data sequence from the reception data input terminal 21 and the reference unique word to output the compared result, a synchronization judgment circuit 23 which detects a frame position based on the compared result concerned, a frame position output terminal 24 which outputs the detected frame position, and a checked result output terminal 29

which outputs the compared result of the unique word detector 22.

[0060] The unique word detector 22 is provided with an input buffer 25 which buffers a received data sequence from the reception data input terminal 21 to output a candidate of unique data, a unique word generator 27 which generates a reference unique word, and a comparator 26 which compares both to output a compared result (for example, exclusive OR). The input buffer 25 cuts out data equal to the unique word length from the data buffered at every predetermined timing to supply it to the comparator 26 and also shifts a cutting out position of data by one bit sequentially at every same timing. Incidentally, the data output sequence (bit output sequence) from the input buffer 25 and the unique word generator 27 is in the forward direction on time axis (FIFO) in the first frame synchronization code detector or in the opposite direction on time axis (LIFO) in the second frame synchronization code detector, so that it is necessary to adopt a different composition for each unique word generator, but to avoid the explanation to become complicated in this embodiment, the composition shown in FIG. 12 is made a representative example. Also, in FIGs. 10A to 10M, in order to make the comparison of each data comprehensible, the data in the opposite direction on time axis is transformed into data in the forward direction on time axis.

[0061] The first frame synchronization code detector 32 of the above mentioned composition detects the frame synchronization code from the received data sequence supplied in the forward direction on time axis to output the first frame position 37 shown in FIG. 10C. On the one hand, in synchronization established state, the unique word generator 27 inside of the first frame synchronization code detector 32 generates the reference unique word in the forward direction shown in FIG. 10D, and the first checked result 40 shown in FIG. 10E is generated by checking the reference unique word and the received data sequence.

[0062] In the example of FIG. 10, four bits from the fifth bit S5 to the eighth bit S8 are lost because of data loss, but code error other than data loss has not occurred, thereby the first checked result FIG. 10E from the first bit S1 to the fourth bit S4 is set "0" correctly. However, beyond the fourth bit, when the j -th bit S_j agrees with the $(j-4)$ -th bit S_{j-4} ($9 \leq j \leq N$), the checked result becomes "0", and when they are in disagreement, it becomes "1", so that bits beyond the fourth bit are expressed by "?" in the figure which indicates indetermination.

[0063] On the other hand, the second frame synchronization code detector 33 performs the similar operation as the first frame synchronization code detector 32 described above except detecting the frame synchronization code in the opposite direction on time axis. Therefore, the second frame position 38, the reference unique word in the opposite direction, and the second checked result 41, as shown in FIGs. 10F to 10H, can be obtained. In the example in FIG. 10, code error other

than data loss has not occurred, thereby the second checked result FIG. 10H from the N -th bit S_N to the ninth bit S9 is set "0" correctly, but before the ninth bit when the j -th bit S_j agrees with the $(j-4)$ -th bit S_{j-4} ($5 \leq j \leq 8$), the second checked result becomes "0", and when they are in disagreement, it becomes "1", so that bits before the ninth bit are expressed by "?". And, in the difference circuit 44, the difference between the first frame position 37 and the immediately following second frame position 38 is determined to supply it to the data loss and data insertion period judgment circuit 34. In the example of FIG. 10, because there is a difference of $N-4$ bits, the data loss and data insertion period judgment circuit 34 judges provisionally that the data loss has occurred.

[0064] Generally, M sequence with low autocorrelation or the like is used for a unique word, so that it is rare that the comparison result between the j -th bit S_j and the $(j-4)$ -th bit S_{j-4} becomes "in agreement" continuously. That is, it is rare that the first checked result 40 after a data loss occurrence position is set to "0" continuously and the second checked result 41 before the data loss occurrence position is also set "0" continuously. On the other hand, as will be apparent from the foregoing description, the first checked result 40 before the data loss occurrence position and the second checked result 41 after the data loss occurrence position are surely set to "0" when there is no code errors other than data loss. The present embodiment, using such a characteristic, presumes the data loss occurrence position by using a boundary point at which the first and second checked results become "in disagreement".

[0065] The point at which the checked result becomes "1" for the first time beyond the data loss occurrence position changes depending on the autocorrelation of a unique word, so that various situations as described below are considered.

D-1. Presumption example 1

[0066] A first checked result example (1) shown in FIG. 10I and a second checked result example (1) shown in FIG. 10J are obtained by assuming that S4 is not equal to S8 and S5 is not equal to S9, and the first start position (immediately after the fourth bit S4) from which there starts a check disagreement subsequent to a check agreement period longer than a predetermined length viewed the first checked result example (1) in the forward direction on time axis agrees with the second start position (immediately before the ninth bit S9) from which there starts a check disagreement subsequent to a check agreement period longer than a predetermined length viewed the second checked result example (1) in the backward direction on time axis. Therefore, it can judge finally that a data loss of a presumed loss length (four bits in this case) has occurred at the position from the fifth bit S5 to the eighth bit S8, that is, at the position between the fourth bit S4 and the fifth bit S5 in the

received data sequence of FIG. 10B. Incidentally, the presumed loss length can be obtained by calculating the difference between the frame length information (N) and the output (N-4) of the difference circuit 44.

[0067] By the way, because the presumed loss length is 4 bits and the presumed loss position is in the position from the fifth bit S5 to the eighth bit S8, as shown by hatching in FIG. 10K, the received data sequence with correct length can be reproduced by inserting the lost frame synchronization code and/or information data to the period equal to four bits from the fifth bit S5 to the eighth bit S8. However, it is actually impossible to reproduce the contents of the lost information data correctly on the reception side, so that in the present embodiment, when the lost data are information data, dummy data with the same length as that of the lost data are inserted into the period concerned. The processing of inserting the lost frame synchronization code and/or dummy data is performed by a dummy data insertion and deletion circuit 42 in Composition 2 and 4 (refer to FIG. 9).

D-2. Presumption example 2

[0068] Next, a presumption example according to a different assumption will be explained.

[0069] FIGs. 11A to 11M show only a part of the frame synchronization code extracted from the received data sequence illustrated in FIG. 6, and FIG. 11A to 11H identical with those of FIGs. 10A to 10M are shown in the upper part of FIGs. 11A to 11P. However, FIGs. 11L to 11P are shown in the lower part of the figure in place of FIG. 10I to 10K. In a first checked result example (2) of FIG. 11L and a second checked result example (2) of FIG. 11M, it is assumed that S4 equals to S8, S5 equals to S9, S3 does not equal to S7, and S6 does not equal to S10, and when viewing in the respective directions on time axis, both of the first start position and the second start position described above exceed the actual data loss positions by one bit, so that the position between the position immediately after the fifth bit S5 and the one immediately before the fourth bit S4 is judged as a presumption loss position. That is, the ambiguity equivalent to two bits occurs in the presumption loss position.

[0070] Thus, when the second start position is prior to the first start position on time axis, there is no choice but to judge finally that the data loss of four bits has occurred in the period from the second start position to the first start position. That is, one of three presumptions of (1) S4 to S7, (2) S5 to S8, and (3) S6 to S9 may be the correct data loss period, but sufficient information has not been obtained to establish one of the three presumptions. When inserting dummy data in such a case, it is safety to process the data loss period as longer period by number of bits corresponding to the degree of above mentioned ambiguity compared with the presumed loss length. In the example of FIGs. 11A to 11M, the presumed loss length is four bits and the presumed

loss position is immediately after one of the third bit S3, the fourth bit S4, and the fifth bit S5, so that the received data sequence with correct length is reproduced by inserting the lost frame synchronization code and/or dummy data into the period equal to six bits from the fourth bit S4 to the ninth bit S9, as shown by hatching in FIG. 10N.

[0071] As described above, the position at which the checked result becomes "1" for the first time beyond the actual data loss occurrence position changes depending on the autocorrelation of unique word. As with many M sequence, when the autocorrelation of unique word is assumed to be "0", the probability in which the first start position described above agrees with the second start position becomes 25%. In addition, the probability in which ambiguity of several bits may occur is as follows;

- (1) one bit : 25%,
- (2) two bits : 18.75%, and
- (3) three bits : 12.5%.

[0072] Therefore, when the ambiguity of three bits or less is made permissible, the data loss period can be presumed with the probability of 80% or more.

D-3. Operation of synchronization judgment circuit 35

[0073] Because Composition 1 is not provided with the data insertion and deletion circuit, even when a data loss period is turned out, it does not operate the received data. Therefore, it only outputs alarm of data loss or informs a data loss period to a subsequent circuit (for example, a decoder corresponding to media coding). However, the first frame position is right as the frame position before data loss and the second frame position is right as the frame position after data loss, so that the frame synchronization position outputted has to be corrected from the first frame position to the second frame position in the synchronization judgment circuit 35. The example of output result of the frame synchronization position in this case is shown in FIG. 11O.

[0074] By the way, in order to make the operation continue quickly in the subsequent frame, it is necessary to correct the reference unique word and first frame position, which are an internal state (internal data) of the first frame synchronization code detector 32, for its purpose, it is very effective to initialize the internal state of the first frame synchronization code detector 32 according to an output result of the synchronization judgment circuit 35 as shown in Composition 3.

[0075] On the other hand, Composition 2 is provided with the data insertion and deletion circuit 42, so that the received data sequence with correct length (corrected received data sequence) can be reproduced by inserting dummy data described above. Therefore, the synchronization judgment circuit 35 always outputs the first frame position as the correct frame position. The example of the output result of the frame synchroniza-

tion position is shown in FIG. 10P. In this case, in order to make the operation continue quickly in the subsequent frame, it is necessary to correct the reference unique word and second frame position, which are an internal state of the second frame synchronization code detector, for its purpose, it is very effective to initialize the internal state of the second frame synchronization code detector 33 according to an output result of the synchronization judgment circuit 35 as shown in Composition 4.

[0076] Incidentally, when applying to neither of the following conditions, the provisional judgment result is changed with the understanding that not the data loss but data insertion, as will hereinbelow be described, has occurred to perform the operation corresponding to data insertion;

- (3) the first start position agrees with the second start position, and
- (4) the second start position is prior to the first start position on time axis.

E. Operation when only data insertion occurs

[0077] Next, the operation of the present embodiment when only data insertion in packet units has occurred (when the code error other than data insertion has not occurred) will be explained.

[0078] FIGs. 13A to 13K shows only a portion of a frame synchronization code extracted from the received data sequence illustrated in FIG. 6. There are shown in the upper part of the figure a received data sequence FIG. 13A without code error, a received data sequence FIG. 13B in which data loss has occurred in a frame, the first frame position FIG. 13C in the forward direction to the received data sequence FIG. 13B, reference unique words FIG. 13D in the forward direction on time axis, the first checked result FIG. 13E in the forward direction to the received data sequence FIG. 13B, the second frame position FIG. 13F in the backward direction to the received data sequence FIG. 13B, reference unique words FIG. 13G in the backward direction on time axis, and the second checked result FIG. 13H in the backward direction to the received data sequence FIG. 13B. In the example shown in this embodiment, as is evident from the received data sequence FIG. 13B, four bits data (SA, SB, SC, and SD) are inserted between the fourth bit S4 and the fifth bit S5.

[0079] When such received data sequence FIG. 13B is input from the input terminal 31, in the first frame synchronization detector 32, a frame code is detected from the received data sequence in the forward direction on time axis to output the first frame position 37, as shown in FIG. 13C. The first frame synchronization code detector 32 has established the synchronization stably using the state transfer of FIG. 3, and in the synchronization established state, the unique word generator inside of the first frame synchronization code detector 32 gener-

ates a reference unique word in the forward direction shown in FIG. 13D. The first frame synchronization detector 32 generates a first checked result 40, as shown in FIG. 13E, by checking the reference unique word in the forward direction and the received data sequence. In the example of FIG. 13A to 13K, data of four bits (SA, SB, SC, and SD) is inserted between the fourth bit S4 and the fifth bit S5, but the code error other than a data insertion has not occurred, so that the first checked result 40 is set "0" correctly until the fourth bit S4. But when SA and S5, SB and S6, SC and S7, SD and S8, and S_j and S_{j-4} ($9 \leq j \leq N$) are in agreement, the first checked result 40 after the fourth bit S4 is set "0", and when in disagreement, it is set "1", so that the bits after the fourth bit S4 are expressed by "?" which indicates indetermination.

[0080] Furthermore, the second frame synchronization code detector 33 performs the similar operation as the first frame synchronization code detector 32 described above except detecting the frame synchronization code in the opposite direction. Thereby, there are obtained the second frame position 38, reference unique words in the opposite direction, and the second checked result 41, as shown in FIGs. 13F to 13H. In the example of FIG. 13A to 13K, the code error other than a data insertion has not occurred, so that while the second checked result 41 from the N-th bit S_N to the ninth bit S9 is set "0" correctly, when SA and S1, SB and S2, SC and S3, and SD and S4 are in agreement, the second checked result 41 before the ninth bit S9 is set "0", and when in disagreement, it is set "1", so that the bits before the ninth bit S9 are expressed by "?" which indicates indetermination.

[0081] And, in the difference circuit 44, the difference between the first frame position 37 and the immediately following second frame position 38 is determined to supply it to the data loss and data insertion period judgment circuit 34. In the example of FIG. 13A to 13K, there is a difference of N+4 bits, so that the data loss and data insertion period judgment circuit 34, at first, judges provisionally that the data loss has occurred. However, this case is applicable to neither of (3) or (4) described above, so that the provisional judgment result is changed with the understanding that the data insertion has occurred. The change process of this provisional judgment will be explained hereinafter in a concrete example.

[0082] Because the data (SA, SB, SC, and SD) placed in the bit positions of a unique word for data insertion are unrelated to the unique word, it is rare that SA and S5, SB and S6, SC and S7, and SD and S8 are all in agreement and SA and S1, SB and S2, SC and S3, and SD and S4 are also in agreement. Therefore, it is rare that the first checked result 40 after the data insertion occurrence position and the second checked result 41 before the data insertion occurrence position are both continuously set to "0".

[0083] On the other hand, both of the first checked

result 40 before the data insertion occurrence position and the second checked result 41 after the data insertion occurrence position are always set to "0", when there is no code error except data insertion. By using such a characteristic, the period in which a data insertion has occurred (data insertion occurrence period) can be presumed according to a boundary point at which two checked results become in disagreement.

[0084] The point at which the checked result becomes "1" for the first time in a data insertion occurrence period changes depending on the inserted data and unique word, so that various situations as described below are considered.

E-1. Presumption example 3

[0085] A first checked result example (1) shown in FIG. 13I and a second checked result example (1) shown in FIG. 13J are obtained by assuming that S5 is not equal to SA and S4 is not equal to SD, and the length from the first start position (immediately after the fourth bit S4) from which there starts a check disagreement subsequent to a check agreement period longer than a predetermined length viewed the first checked result example (1) in the forward direction on time axis to the second start position (immediately before the fifth bit S5) from which there starts a check disagreement subsequent to a check agreement period longer than a predetermined length viewed the second checked result example (1) in the backward direction on time axis becomes four bits. The four bits agree with a presumed insertion length, so that the provisional judgment is changed such that a data insertion of a presumed insertion length (in this case, four bits) has occurred in the position from SA to SD, that is, in the position (presumed insertion position) from the fifth bit to the eighth bit in the received data sequence of FIG. 13B. Incidentally, the presumed insertion length can be obtained by calculating the difference between the output of the difference circuit 44 ($N+4$) and the frame length information (N).

[0086] In addition, because the presumed insertion length is four bits and the presumed insertion position is the one from SA to SD, as shown in FIG. 13K, the received data sequence with correct length can be reproduced by deleting the data in a period equivalent to four bits of SA to SD. The dummy data insertion and deletion circuit 42 (refer to FIG. 9) performs the process. In the example illustrated in FIG. 13A to 13K, because the data insertion period agrees with the presumed insertion period completely, the corrected receive data sequence in which not only length but also contents are correct can be obtained by deleting the data.

E-2. Presumption example 4

[0087] Next, a presumption example according to a different assumption will be explained.

[0088] FIG. 14A to 14P shows only a part of the frame synchronization code extracted from the received data sequence illustrated in FIG. 6, and FIGs. 14A to 14K identical with those of FIGs. 13A to 13K are shown in the upper part of FIGs. 14A to 14P. However, FIGs. 14L to 14P are shown in the lower part of the figure in place of FIGs. 13I to 13K. A first checked result example (2) of FIG. 14L and a second checked result example (2) of FIG. 14M are obtained by assuming that S5 equals to SA, S6 does not equal to SB, and S4 does not equal to SD, and as will be apparent from the assumption, the first start point is set to a position exceeding the actual data insertion position by one bit. Therefore, in FIG. 14B, the position between the position immediately after the fifth bit SA and the position immediately before the ninth bit S5 is presumed as the presumed insertion position. That is, the presumed data insertion period length becomes three bits which are shorter by one bit than four bits of the presumed insertion length. The synchronization judgment circuit 35 can not determine the actual data insertion occurrence position, so that the ambiguity equivalent to one bit occurs in the presumed insertion position.

[0089] In such a case, there is no choice but to judge finally that the data insertion of the insertion presumed length (in this case, four bits) has occurred in any position including from the first start position to the second start position. That is, either of (1) SA to SD or (2) SB to S5 is the correct data insertion period, but the sufficient information to decide either has not been obtained. Here, an example (2) of insertion data deletion which adopts (2) described above is shown in FIG. 14N. In this example (2) of insertion data deletion, as shown by hatching, data SA remains in the position of the fifth bit S5 and, instead, the content of the fifth bit S5 is lost.

[0090] As mentioned above, it is assumed that S5 equals to SA in this example, so that the corrected unique word is set to a right result, but an information data peripheral to S5 is resulted in replacement of the inserted data. Thus, when the length from the first start position to the second start position is shorter than a presumed insertion length, a part of the contents of the information data is resulted in incorrect, while the length and unique word of the corrected received data sequence are right.

[0091] As previously stated, the position in which the checked result becomes "1" for the first time in a data insertion period changes depending on the inserted data and unique word. When the cross-correlation between the unique word and the inserted data is assumed to be 0, the probability in which the period from the first start position to the second start position agrees with the presumed insertion length will become 25%. In addition, the probability in which the ambiguity of several bits will produce is as follows;

- (1) one bit : 25%
- (2) two bits : 18.75%

(3) three bits : 12.5%

[0092] Therefore, when the ambiguity less than three bits is made permissible, the data presumption period can be presumed with a probability more than 80%.

E-3. Operation of the synchronization judgment circuit 35

[0093] As with the explanation in A-4-3, the synchronization judgment circuit 35 corrects the frame synchronization position output. As a result, the frame synchronization position output from the synchronization judgment circuit 35 becomes the position shown in FIG. 14O in Composition 1 and also the position shown in FIG. 14P in Composition 2. This allows the operation to be continued quickly in a following frame. Incidentally, it will be appreciated that the internal state of each frame synchronization code detector may be initialized according to the output result of the synchronization judgment circuit 35.

[0094] While the present embodiment has been described, it works effectively when only a usual code error occurs and when only a data loss/insertion in packet units generates.

F. When a data loss overlaps on a usual code error

[0095] There has been described a case in which only a usual code error or only a data loss/insertion in packet units occurs, but in actual application, a difference kind of code error often overlaps on a usual one. The operation in such a case will be described with reference to FIGs. 15A to 15P and FIGs. 16A to 16P.

[0096] In the example shown in FIGs. 15A to 15P, as with in FIG. 10A to 10M, a data loss of four bits from the fifth bit S5 to the eighth bit S8 has occurred, and in addition, usual code errors are overlapped at the third bit S3 and the tenth bit S10. Because of those usual code errors, the first checked result and the second checked result become "1" for the first time at the third bit S3 and the tenth bit S10, respectively. Thus, the first start position becomes immediately after the second bit S2 and the second start position becomes immediately before the eleventh bit S11.

[0097] When usual code errors are overlapped on a data loss in this way, the data loss corresponds to neither of (3) or (4) and there is a probability that the data loss may be interpreted as data insertion accidentally.

[0098] To solve this problem, the following countermeasures are considered;

(5) the embodiment is not applied to a data insertion,

(6) a data loss and data insertion are enabled to be distinguished by adding a frame number to a frame synchronization code,

(7) data loss and data insertion are enabled to be

distinguished by adding limitation to a length of data loss/insertion.

F-1. Countermeasure (5) (Equivalent to claim 5)

[0099] The countermeasure (5) functions only when a usual code error has overlapped on a data loss. When it is taken into account that cell loss in ATM transmission and packet loss on an Internet are either data loss phenomena and the occurrence probability of data loss is substantially higher than that of data insertion in a multimedia multiplexing, it is considered that if this embodiment functions effectively only when a usual code error overlaps on a data loss, sufficiently high practicality can be obtained.

[0100] Here, the operation adopted the countermeasure (5) will be explained with reference to FIGs. 15A to 15P.

[0101] In the example shown in FIGs. 15A to 15P, the first start position is prior to the second start position on time axis, so that it is recognized that a data loss may occur somewhere in this period, but a data loss occurrence position can not be specified. Alternatively, the data loss occurrence position is assumed to insert a dummy data into the position. However, in the example (1) of dummy data insertion shown in FIG. 15K, dummy data are inserted into the period between the fifth bit S5 and the eighth bit S8 based on the assumption that a data loss has occurred immediately after the fourth bit S4. This dummy data insertion position is adventitiously the right position.

[0102] On the other hand, the example (2) of dummy data insertion shown in FIG. 15L assumes that a data loss has occurred immediately after the sixth bit S6, and inserts a dummy data into the period from the seventh bit S7 to the tenth bit S10 by mistake. When usual code errors overlap on a data loss in this way, somewhat of errors may occur, but there are maintained the advantages that a frame synchronization can be retained stably and a corrected received data with right length can be obtained.

F-2. Countermeasure (6) (equivalent to claim 6)

[0103] Moreover, the countermeasure (6) can distinguish a data loss and data insertion by using a frame number together. Thus, it functions effectively to both cases in which a usual code error and data loss are overlapped and a usual code error and data insertion is overlapped. In practice, many multimedia applications add the frame number, so that this countermeasure can often be adopted without causing the data redundancy. The operation applied this countermeasure concretely will be described hereinafter.

[0104] In the example shown in FIGs. 15A to 15P, a frame number corresponding to a second frame position immediately after a first frame position is larger by one than a frame number corresponding to the first

frame position in the left of the figure. This means that the second frame position is acquired prior to the first frame position for the same frame, that is, a data loss has occurred in the frame concerned. Thus, although the first start position is prior to the second start position on time axis, it can be judged that not data insertion but data loss has occurred.

[0105] On the other hand, in the example shown in FIGs. 16A to 16P (example of data insertion), a frame number corresponding to a first frame position and a frame number corresponding to its immediately following second frame position are in agreement. This means that the first frame position is acquired prior to the second frame position for the same frame, that is, a data insertion has occurred in the frame concerned. Thus, it can be judged that not data insertion but data loss has occurred.

F-3. Countermeasure (7) (equivalent to claim 7)

[0106] Furthermore, when a packet length is smaller sufficiently than a frame length, a data loss/data insertion can be distinguished by adding limitation to a presumed loss length and presumed insertion length (countermeasure (7)). For example, when a permissible presumed loss length (a first threshold value) and a permissible presumed insertion length (a second threshold value) are both set to a half of the frame length, an effect equivalent to the countermeasure (6) can be obtained.

[0107] Incidentally, the concrete insertion method of the dummy data in countermeasure (6) and (7) is as similar to the method in the countermeasure (5) described above.

G. When data insertion overlaps on usual code error

[0108] Next, the processing when a data insertion overlaps on a usual code error will be described with reference to FIGs. 16A to 16P. Incidentally, in FIGs. 16A to 16P, as for the data insertion phenomenon, as with the phenomenon in A-5, it is assumed that a data insertion of four bits will occur between the fourth bit S4 and the fifth bit S5 and also usual code errors will generate in the third bit S3 and the fifth bit S5.

[0109] As is evident from FIGs. 16A to 16P, the length of presumed data insertion period is seven bits longer by three bits than the actual length (in this case, four bits) according to the code error. It is recognized that a data insertion may occur somewhere in this period, but a data insertion occurrence position can not be specified. Accordingly, the data insertion occurrence position should be assumed to delete data. In the example (1) of inserted data deletion shown in FIG. 16K, the data in the period from the fifth bit to the eighth bit (SA to SD) are deleted. This is the accidental data deletion in the right period.

[0110] On the other hand, in the example (2) of insertion data deletion shown in FIG. 16L, it is assumed that

a data insertion has occurred, so that data of the period from the third bit S3 to the sixth bit S6 are deleted. As a result, in the example (2) of insertion data deletion, the third bit S3 and the fourth bit S4 corresponding to the correct data are deleted, and on the contrary, the inserted data SC and SD remain. When a usual code error overlaps on a data insertion in this way, somewhat of errors may occur, but there are maintained the advantages that a frame synchronization can be retained stably and a corrected received data with right length can be obtained.

H. In a case of variable length frame

[0111] Incidentally, a fixed length frame is presupposed to be used in the above mentioned explanation, but when a frame length information is included in a frame synchronization code, the present embodiment can be operated like the explanation above, even when a variable length frame is used. In this case, a frame synchronization code detector shown in FIG. 18 may be used. The frame synchronization code detector shown in FIG. 18 is provided with a frame length detector 18 (refer to FIG. 4), detects the frame length information in the received data sequence from the received data input terminal 21 with this frame length detector 18, supplies the frame length information detected to a synchronization judgment circuit 23, and outputs it through a frame length information output terminal 9. And, the symbol 8 in FIG. 18 designates a frame number detector, which detects a frame number in the received data sequence from the received data input terminal 21 to output it through a frame number output terminal 10.

[0112] Furthermore, even when the frame length information is not included in the received data sequence, when a unique word which can be detected in the opposite direction on time axis is set up appropriately, the operation like the embodiment described above can be achieved. There is shown a composition of the frame synchronization code detector in this case in FIG. 17.

[0113] In addition, when there is used a pseudo fixed length frame with a pointer indicating the head position of the information data in a portion of the frame synchronization code with fixed length frame composition to the information data of the variable length frame composition, the operation like the embodiment described above can be achieved without adding special means.

I. When data loss/insertion occur in a general length

[0114] In the explanation described above, it is assumed that the data loss/insertion occurs in multiples of the arrangement interval of a unique word, but the present embodiment works normally even when this assumption is not come into existence. The present embodiment detects the position and length (period) of the data loss/insertion by determining the frame position in the forward and backward direction on time axis

and also by checking the reference unique word and the received data sequence. In the above mentioned checking process, even when a checking object following the position at which the data loss/insertion has occurred is not a unique word but an information data, a check disagreement may occur as well, so that the present embodiment operate normally even when the data loss/insertion does not occur in multiples of the arrangement interval of the unique word.

[The second embodiment]

[0115] FIG. 19 is a block diagram showing the composition of the frame synchronization circuit according to another embodiment. When comparing this composition with the one shown in FIG. 8, the second frame synchronization code detector 33 and the difference circuit 44 are removed, a data loss and data insertion period judgment circuit 54 is provided in place of the data loss and data insertion period judgment circuit 34, and a synchronization judgment circuit 55 is provided in place of the synchronization judgment circuit 35.

[0116] The data loss and data insertion period judgment circuit 54 accumulates evaluation values of the checked result 40 and judges whether a data loss or data insertion has occurred based on whether the accumulation result exceeds the predetermined threshold value. For example, the evaluation value for "0" (agreement) of the checked result 40 can be set as "-1" and for "1" (disagreement) as "+2", and the predetermined threshold value can be set as "5". However, the accumulation result does not become less than "0".

[0117] Next, there will be explained the operation of this embodiment when a code error occurs with reference to FIGs. 20A to 20G. The frame synchronization code detector 32, as with the first embodiment, checks the reference unique word and received data sequence in the forward direction to output the checked result 40, as shown in FIG. 20E. Incidentally, the contents of FIGs. 20A to 20E are similar to those of FIGs. 7A to 7E.

[0118] The evaluation values corresponding to the checked result 40 are accumulated in the data loss and data insertion period judgment circuit 54. The checked result 40 keeps "0" until the third bit S3 in FIGs. 20A to 20G, so that the evaluation value is "-1" and the accumulation result keeps "0". This is because the accumulation result never becomes less than "0" as described above.

[0119] When the checked result 40 becomes "1" at the fourth bit S4, the evaluation value becomes "2" and the accumulation result also becomes "2". Next, when the checked result 40 becomes "0" at the fifth bit S5, the evaluation value becomes "2" and the accumulation result becomes "1". Next, when the checked result 40 becomes "1" at the sixth bit S6, then the evaluation value becomes "2" and the accumulation result becomes "3". The checked result 40 keeps "0" continuously since the seventh bit S7, so that the accumulation

result is decremented by "1" and returns to "0" at the ninth bit S9. In the example described above, because the accumulation result never exceeds the threshold value "5", the judgment result of FIG. 20G always keeps "0".

[0120] Next, there will be explained the operation when a data loss has occurred in the present embodiment with reference to FIGs. 21A to 21H. FIG. 21A shows a received data sequence without code error, and FIG. 21B shows a received data sequence in which a data loss has occurred in a frame. FIG. 21E shows both checked results. In FIG. 21E, the checked results from the first bit S1 to the fourth bit S4 are "0". The checked results after the fifth bit S5 become random values corresponding to the contents of the data sequence.

[0121] One example of this random checked results are shown in FIG. 21F. Also, the accumulation result of evaluation value to this checked result is shown in FIG. 21G. When a data loss has occurred, the checked result 40 never returns to continuous "0", so that the accumulation result exceeds a threshold value at a certain point, and the judgment result shown in FIG. 21H becomes "0". When this judgment result is transmitted to the synchronization judgment circuit 55, there is detected "synchronous error" caused by data loss.

[0122] According to the detected result, the synchronization judgment circuit 55 stops the output of the frame position, and outputs an instruction to the frame synchronization code detector 32 to make detect the unique word once again.

[0123] Furthermore, even when a data insertion has occurred in the present embodiment, the phenomenon completely similar to that described above may occur. Thus, the judgment result becomes "1" as in the case when the data loss has occurred, so that the output of the frame position may be stopped to detect the unique word once again.

[0124] It is preferred that the threshold value in the present embodiment is set to a value which can detect a slightly longer error than an assumed one generally occurred in a transmission channel. However, even when the threshold value is set in this manner, when an error occurs over a longer interval than assumed, the judgment result turns to "1" even though a data loss or data insertion has not occurred. In such a case, the occurrence of such phenomenon means that the state of transmission channel is substantially deteriorated, so that even though a frame synchronization is retained, to obtain a correct received data can not be expected.

Therefore, it is considered that a practical problem may not occur according to the judgment result of "1" in such a state.

55 Claims

1. A frame synchronization circuit used on a reception side of a data transmission system adopted a frame

composition in which a frame synchronization code is positioned in a frame scatteredly, said frame synchronization circuit comprising;

- a frame synchronization code detector detecting the frame synchronization code from a received data sequence to output a frame position, and outputting a checked result by checking the frame synchronization code detected and a correct frame synchronization code; and a data loss and data insertion period judgment circuit presuming whether a data loss or data insertion has occurred in said received data sequence according to said checked result.
2. A frame synchronization circuit according to claim 1 wherein:
- (a) said frame synchronization code detector comprising;
- a first frame synchronization code detector detecting a frame synchronization code by checking with a correct frame synchronization code in the forward direction on time axis for a received data sequence to output a detected position as a first frame position and outputting the checked result as a first checked result; and
- a second frame synchronization code detector detecting a frame synchronization code by checking with a correct frame synchronization code in the backward direction on time axis for said received data sequence to output a detected position as a second frame position and outputting the checked result as a second checked result;
- (b) said data loss and data insertion period judgment circuit comprising;
- a difference circuit detecting a length from said first frame position to said immediately following second frame position; and a frame length information output means outputting a frame information;
- said data loss and data insertion period judgment circuit presuming a data loss period or data insertion period included in said received data sequence according to said frame length information, a length output from said difference circuit, said first checked result, and said second checked result;
- (c) and further comprising;
- a synchronization judgment circuit deter-

mining and outputting a frame synchronization position according to said first frame position, said second frame position, and a presumed result of said data loss and data insertion period judgment circuit.

3. A frame synchronization circuit according to claim 2 further comprising:

a dummy data insertion and deletion circuit inserting a dummy data to a presumed data loss period and deleting a data from a presumed data insertion period for said received data sequence to output as a corrected received data sequence.

4. A frame synchronization circuit according to claim 2 wherein:

said first frame synchronization code detector and said second frame synchronization code detector use a frame synchronization position output from said synchronization judgment circuit as an initial value, when a data loss period or data insertion period is presumed by said data loss and data insertion period judgment circuit.

5. A frame synchronization circuit according to claim 3 wherein:

said first frame synchronization code detector and said second frame synchronization code detector use a frame synchronization position output from said synchronization judgment circuit as an initial value, when a data loss period or data insertion period is presumed by said data loss and data insertion period judgment circuit.

6. A frame synchronization circuit according to any one of claims 2 to 5 wherein:

said data loss and data insertion period judgment circuit, when said frame length information of a frame to be processed is different from a length output from said difference circuit, judges provisionally that a data loss has occurred in the frame;

(1) when a first start position, from which a check disagreement starts, followed by a continuous check agreement period which can be obtained from said first checked result viewed in the forward direction on time axis and is longer than a predetermined length agrees with a second start position, from which a check disagreement

starts, followed by a continuous check agreement period which can be obtained from said second checked result viewed in the backward direction on time axis and is longer than predetermined length, it is finally judged that a data loss of a number of bits corresponding to a difference between said frame length information of a frame to be processed and a length output from said difference circuit has occurred at the position;

(2) when said second start position is prior to said first start position on time axis, it is finally judged that a data loss of said number of bits has occurred in any position in the period from said second start position to said first start position,

in a case which is not applicable to either of (1) and (2), the provisional judgment is changed from data loss to data insertion;

(3) when a length of an period from said first start position to said second start position agrees with a length output from said difference circuit, the period is judged finally to be a data insertion period; and
(4) when the length of an period from said first start position to said second start position is shorter than the length output from said difference circuit, the period of said number of bits including the period is judged finally to be a data insertion period.

7. A frame synchronization circuit according to any one of claims 2 to 5 wherein:

said data loss and data insertion period judgment circuit, when said frame length information of a frame to be processed is different from a length output from said difference circuit, judges provisionally that a data loss has occurred in the frame;

(1) when a first start position, from which a check disagreement starts, followed by a continuous check agreement period which can be obtained from said first checked result viewed in the forward direction on time axis and is longer than a predetermined length agrees with a second start position, from which a check disagreement starts, followed by a continuous check agreement period which can be obtained from said second checked result viewed in the backward direction on time axis and is longer than predetermined length, it is finally judged that a data loss of a number

of bits corresponding to a difference between said frame length information of a frame to be processed and a length output from said difference circuit has occurred at the position;

(2) when said second start position is prior to said first start position on time axis, it is finally judged that a data loss of said number of bits has occurred in any position in the period from said second start position to said first start position; and

(3) when said first start position is prior to said second start position on time axis, it is finally judged that a data loss of said number of bits has occurred in any position in the period from said first start position to said second start position.

8. A frame synchronization circuit according to any one of claims 2 to 5, further characterized in:

that said frame includes a frame number;
that said frame synchronization circuit is used on a reception side of a data transmission system in which a frame number is enabled to be detected on the reception side;
that said data loss and data insertion period judgment circuit, when said frame length information of a frame to be processed is different from a length output from said difference circuit, judges provisionally that a data loss has occurred in the frame;
that executing a first final judgement, when a first start position, from which a check disagreement starts, followed by a continuous check agreement period which can be obtained from said first checked result viewed in the forward direction on time axis and is longer than a predetermined length agrees with a second start position, from which a check disagreement starts, followed by a continuous check agreement period which can be obtained from said second checked result viewed in the backward direction on time axis and is longer than predetermined length, said first final judgement is that a data loss of a number of bits corresponding to a difference between said frame length information of a frame to be processed and a length output from said difference circuit has occurred at the position;
that executing a second final judgement, when said second start position is prior to said first start position on time axis, said second final judgement is that a data loss of said number of bits has occurred in any position in the period from said second start position to said first start position;
that executing a third final judgement, when

said first start position is prior to said second start position on time axis and a frame number indicated by said first frame position and a frame number indicated by said immediately following second frame position are continuous, said third final judgement is that a data loss of said number of bits has occurred in any position in the period from said first start position to said second start position;

that in a case where either of said first, second, and third final judgements are not applicable, the provisional judgment is changed from data loss to data insertion;

that when a length of an period from said first start position to said second start position agrees with a length output from said difference circuit, the period is judged finally to be a data insertion period;

that when the length of an period from said first start position to said second start position is shorter than the length output from said difference circuit, the period of said number of bits including the period is judged finally to be a data insertion period; and

that when the length of an period from said first start position to said second start position is longer than the length output from said difference circuit, it is finally judged that a data insertion of said number of bits has occurred in any position in the period.

9. A frame synchronization circuit according to any one of claims 2 to 5, further characterized in:

that said data loss and data insertion period judgment circuit, when said frame length information of a frame to be processed is different from a length output from said difference circuit and a difference of both is smaller than a predetermined first threshold value, judges provisionally that a data loss has occurred in the frame;

that when a first start position, from which a check disagreement starts, followed by a continuous check agreement period which can be obtained from said first checked result viewed in the forward direction on time axis and is longer than a predetermined length agrees with a second start position, from which a check disagreement starts, followed by a continuous check agreement period which can be obtained from said second checked result viewed in the backward direction on time axis and is longer than predetermined length, it is finally judged that a data loss of a number of bits corresponding to a difference between said frame length information of a frame to be processed and a length output from said difference

circuit has occurred at the position;

that when said second start position is prior to said first start position on time axis, it is finally judged that a data loss of said number of bits has occurred in any position in the period from said second start position to said first start position;

that when said first start position is prior to said second start position on time axis, it is finally judged that a data loss of said number of bits has occurred in any position in the period from said first start position to said second start position;

that said frame length information of the frame and a length output from said difference circuit are different and the length output from said difference circuit is smaller than a predetermined second threshold value, it is judged provisionally that a data insertion has occurred in the frame;

that when a length of an period from said first start position to said second start position agrees with a length output from said difference circuit, the period is judged finally to be a data insertion period;

that when the length of an period from said first start position to said second start position is shorter than the length output from said difference circuit, the period of said number of bits including the period is judged finally to be a data insertion period; and

that when the length of an period from said first start position to said second start position is longer than the length output from said difference circuit, it is finally judged that a data insertion of said number of bits has occurred in any position in the period.

10. A frame synchronization circuit according to claim 1 further comprising:

a synchronization judgment circuit determining and outputting a frame synchronization position according to said frame position and a presumed result of said data loss and data insertion period judgment circuit.

11. A frame synchronization circuit according to claim 10 wherein:

said data loss and data insertion period judgment circuit accumulating a evaluation value of said checked result and judging whether a data loss or data insertion has occurred according to the accumulated result.

FIG. 1A

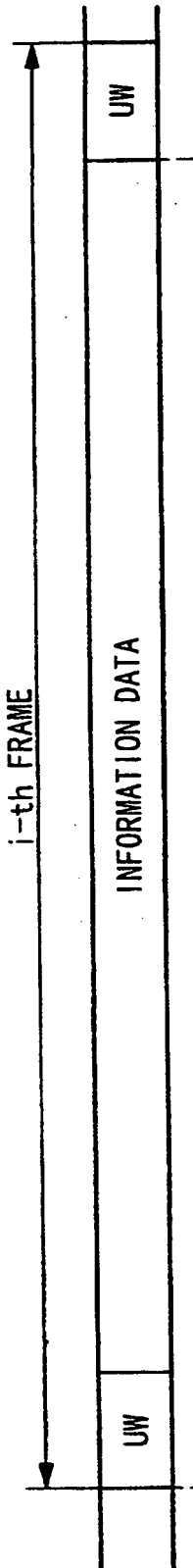


FIG. 1B

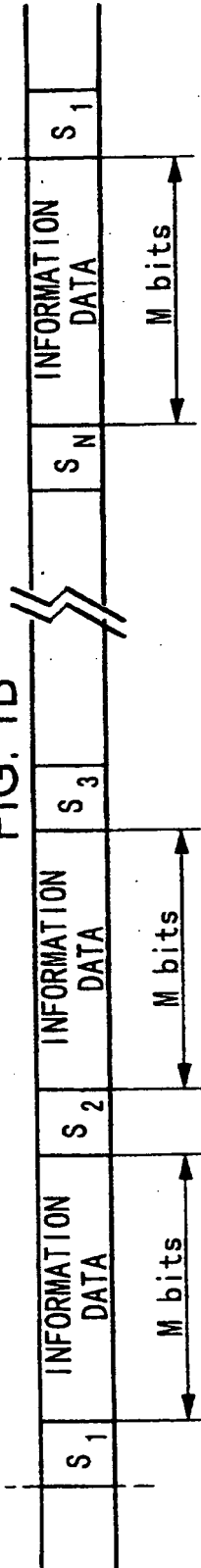


FIG. 1C

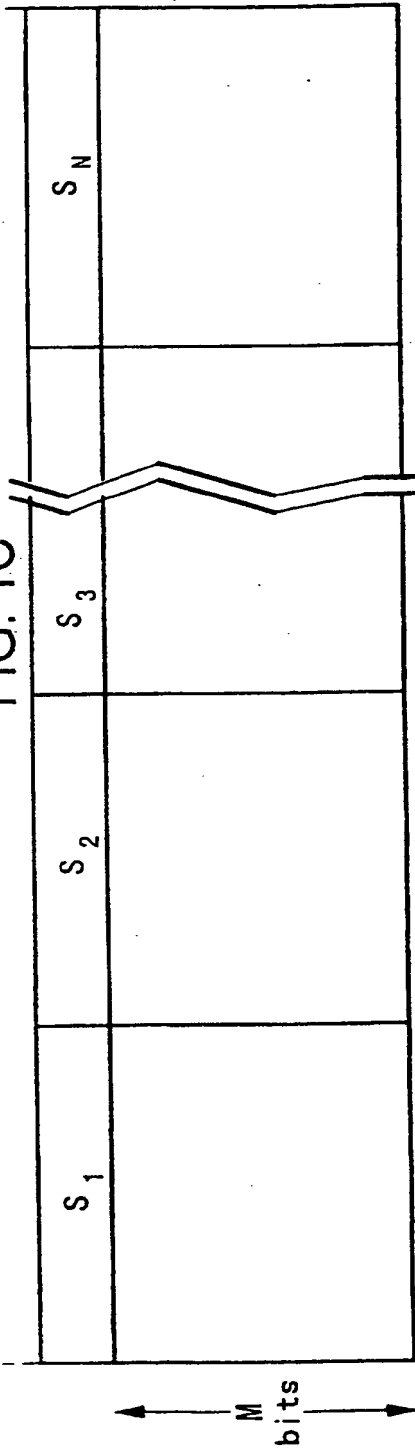


FIG. 1D



FIG. 2

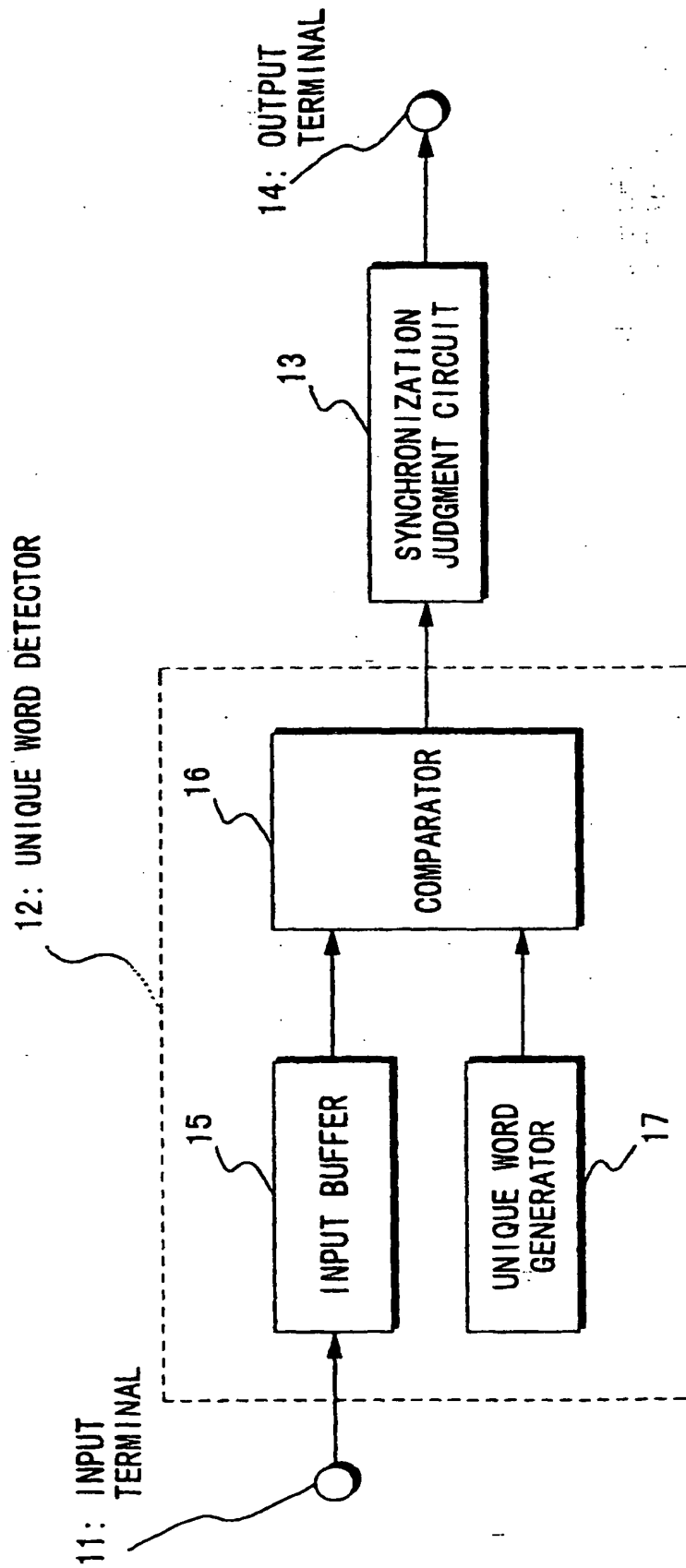


FIG. 3

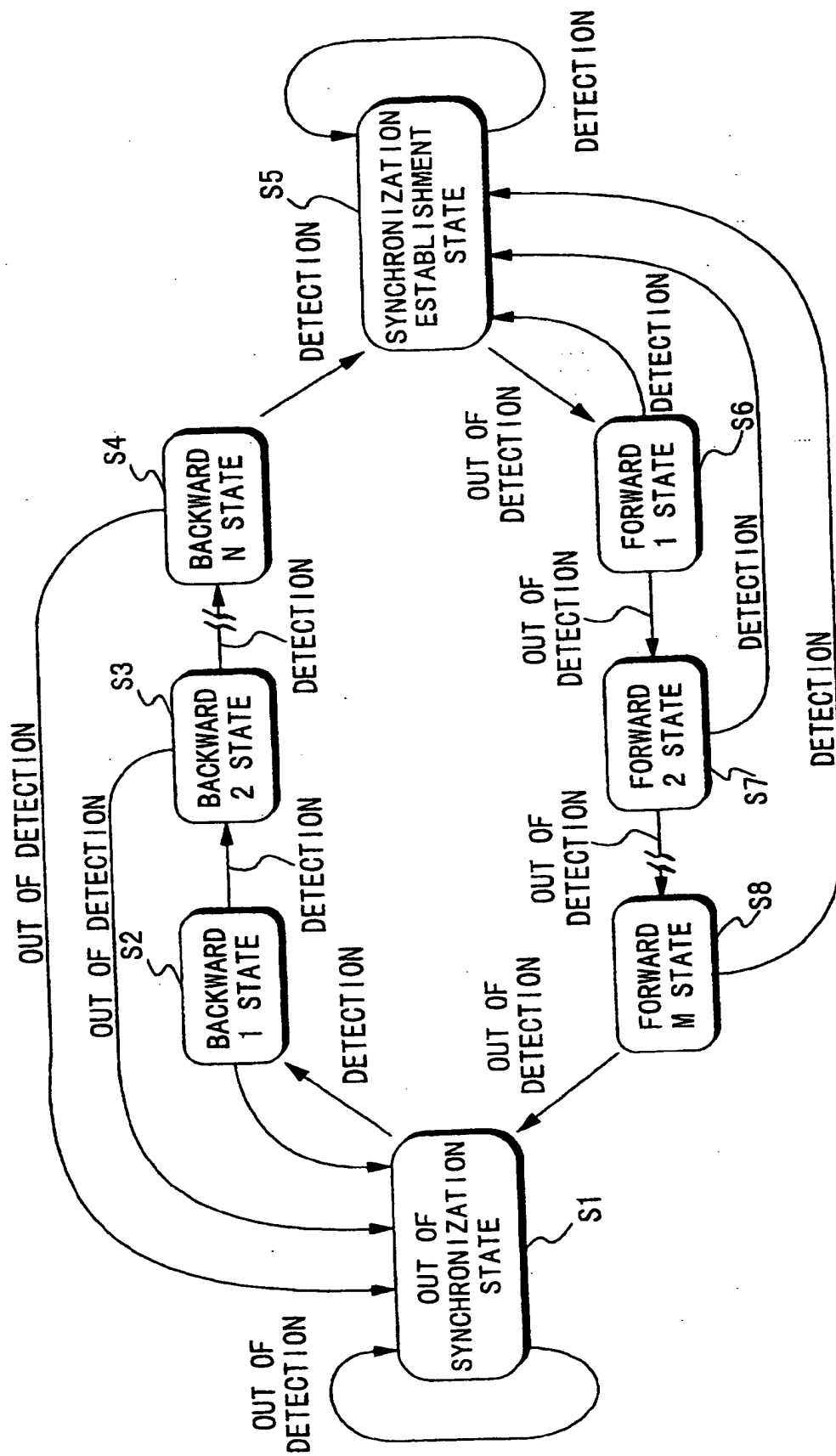


FIG. 4

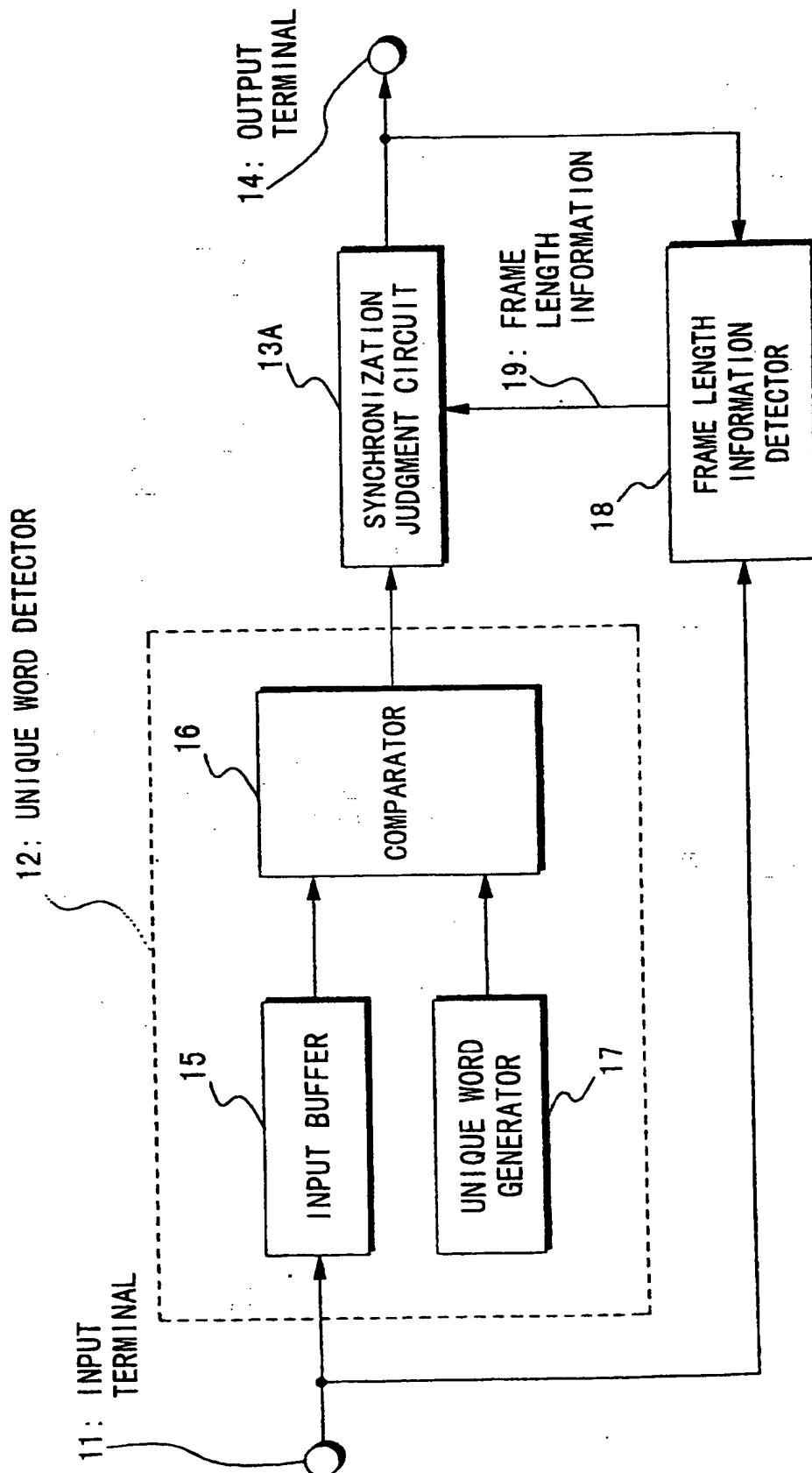


FIG. 5A

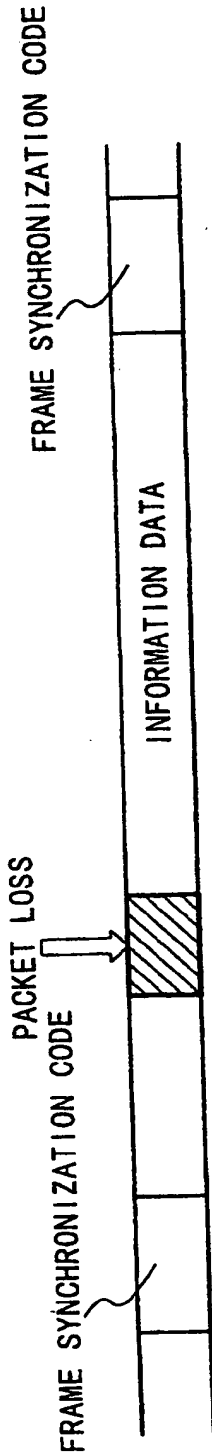


FIG. 5B

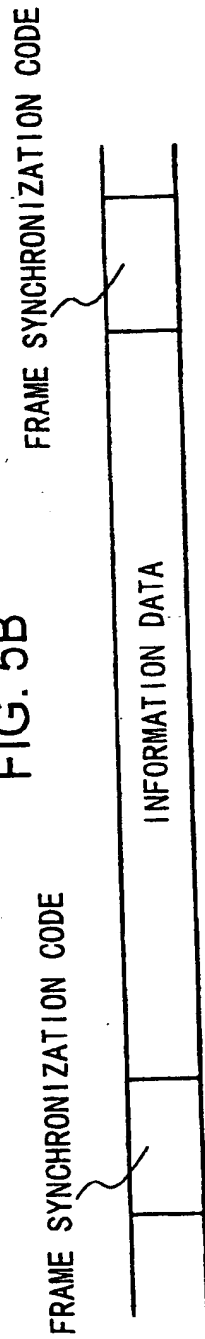


FIG. 5C

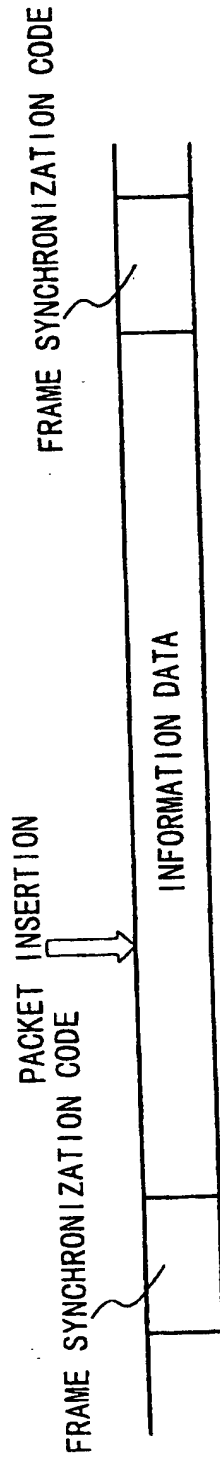


FIG. 5D

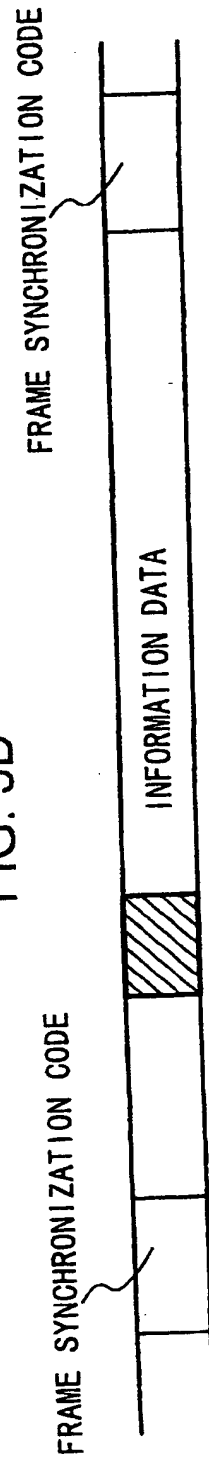


FIG. 6

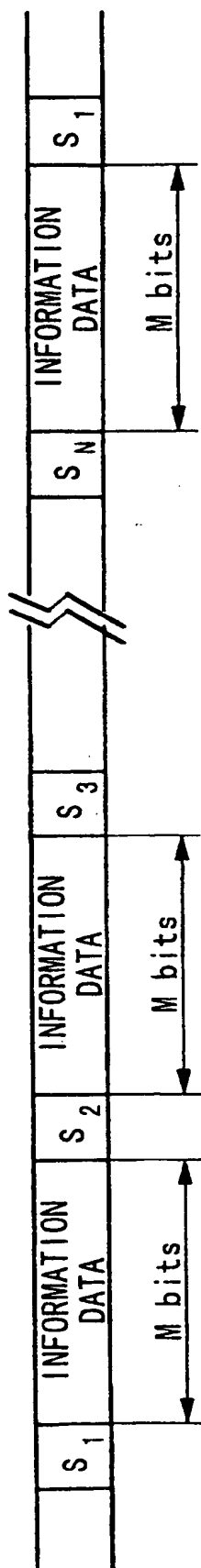


FIG. 7A
RECEIVED DATA SEQUENCE WITHOUT CODE ERROR



FIG. 7B
RECEIVED DATA SEQUENCE WITH CODE ERROR



FIG. 7C
FIRST FRAME POSITION



FIG. 7D
REFERENCE UNIQUE WORD (FORWARD DIRECTION)

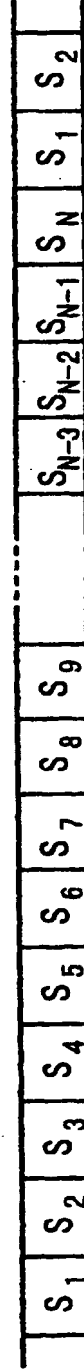


FIG. 7E
FIRST CHECKED RESULT

0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

FIG. 7F
SECOND FRAME POSITION



FIG. 7G
REFERENCE UNIQUE WORD (BACKWARD DIRECTION)

S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉		S _{N-3}	S _{N-2}	S _{N-1}	S _N	S ₁	S ₂
----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------	--	------------------	------------------	------------------	----------------	----------------	----------------

FIG. 7H
SECOND CHECKED RESULT

0	0	0	1	0	1	0	0	0		0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	--	---	---	---	---	---	---

FIG. 8

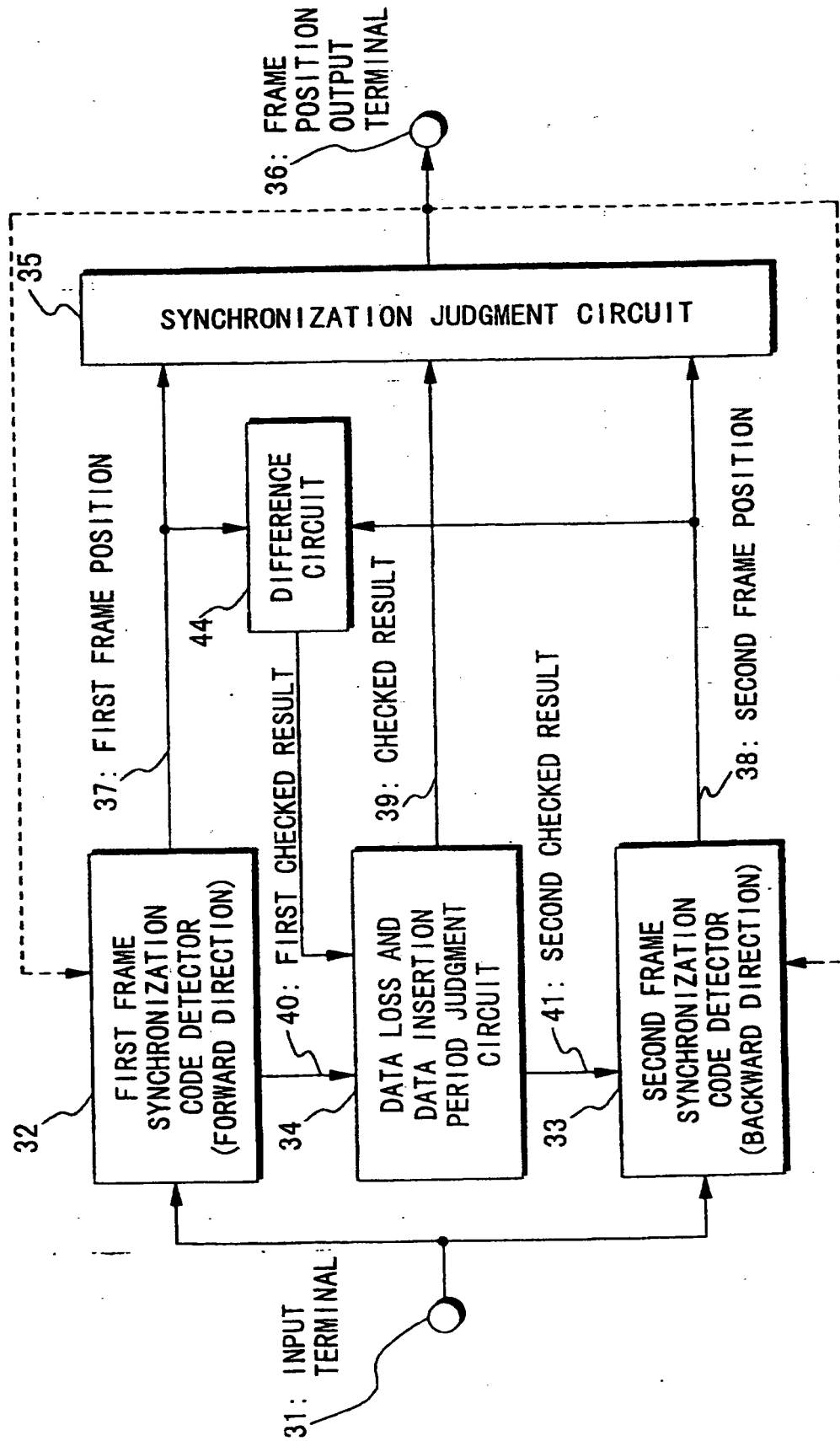


FIG. 9

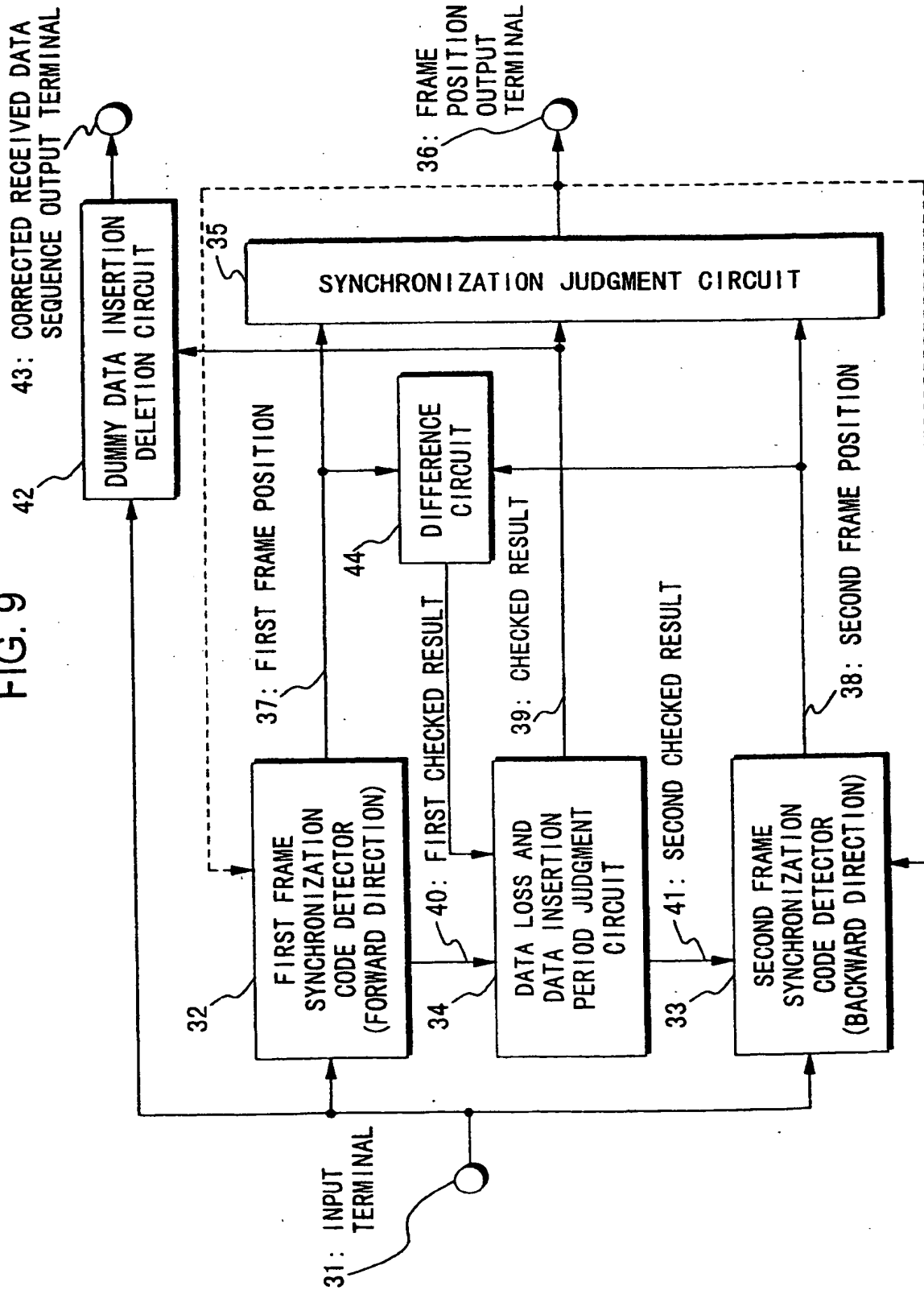


FIG. 10A
RECEIVED DATA SEQUENCE WITHOUT CODE ERROR

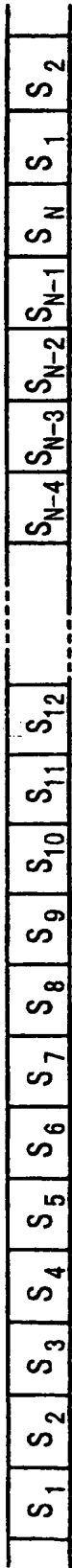


FIG. 10B
RECEIVED DATA SEQUENCE WITH CODE ERROR



FIG. 10C
FIRST FRAME POSITION



FIG. 10D
REFERENCE UNIQUE WORD (FORWARD DIRECTION)



FIG. 10E
FIRST CHECKED RESULT



FIG. 10F
SECOND FRAME POSITION



FIG. 10G
REFERENCE UNIQUE WORD (BACKWARD DIRECTION)

S ₁	S ₂	S ₃	S ₄	S ₉	S ₁₀	S ₁₁	S ₁₂	S ₁₃	S ₁₄	S ₁₅	S ₁₆	S _N	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆
----------------	----------------	----------------	----------------	----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------

FIG. 10H
SECOND CHECKED RESULT

?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---



LOSS OCCURRENCE POSITION
(FOR FOUR BITS)

FIG. 10I
FIRST CHECKED RESULT EXAMPLE (1)

0	0	0	0	1	0	0	1	1	0	1	0	?	?	?	?	?	?	?
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

FIG. 10J

[illegible]

DATA LOSS PRESUMED POSITION

FIG. 10K
DUMMY DATA INSERTION EXAMPLE (1)

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}		S_{N-3}	S_{N-2}	S_{N-1}	S_N	S_1	S_2
--	-------	-------	-------	-------	-------	-------	-------	-------	-------	----------	----------	----------	--	-----------	-----------	-----------	-------	-------	-------

FIG. 10L
FIRST CHECKED RESULT EXAMPLE (2)

	0	0	0	0	0	1	0	1	1	0	1	0	?	?	?	?	?	?
--	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

FIG. 10M
SECOND CHECKED RESULT EXAMPLE (2)

[illegible]

FIG. 11A
RECEIVED DATA SEQUENCE WITHOUT CODE ERROR



FIG. 11B
RECEIVED DATA SEQUENCE WITH CODE ERROR

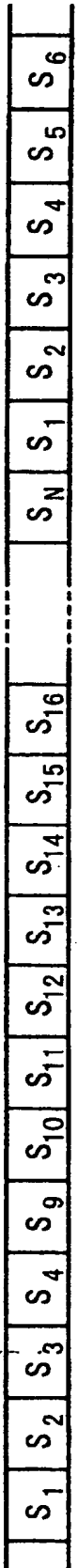


FIG. 11C
FIRST FRAME POSITION

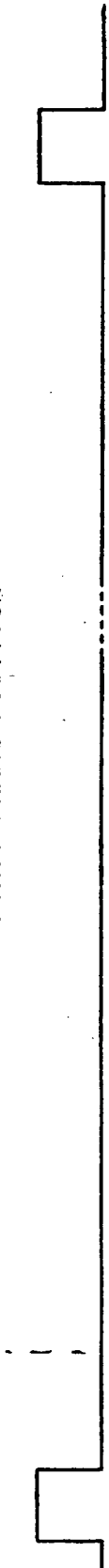


FIG. 11D
REFERENCE UNIQUE WORD (FORWARD DIRECTION)



FIG. 11E
FIRST CHECKED RESULT



FIG. 11F
SECOND FRAME POSITION



FIG. 11G
REFERENCE UNIQUE WORD (BACKWARD DIRECTION)

S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_N	S_1	S_2	S_3	S_4	S_5	S_6
-------	-------	-------	-------	-------	----------	----------	----------	----------	----------	----------	----------	-------	-------	-------	-------	-------	-------	-------

FIG. 11H
SECOND CHECKED RESULT

?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

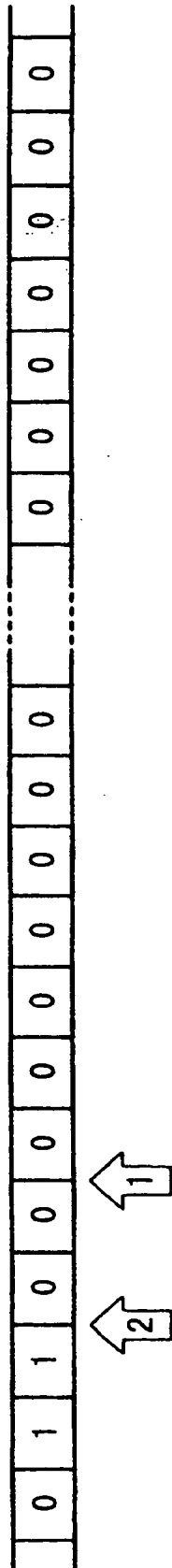


LOSS OCCURRENCE POSITION
(FOR FOUR BITS)

FIG. 11L
FIRST CHECKED RESULT EXAMPLE (2)

0	0	0	0	0	1	0	1	1	0	1	0	?	?	?	?	?	?	?
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

FIG. 11M
SECOND CHECKED RESULT EXAMPLE (2)



DATA LOSS PRESUMED POSITION

FIG. 11N
DUMMY DATA INSERTION EXAMPLE (2)

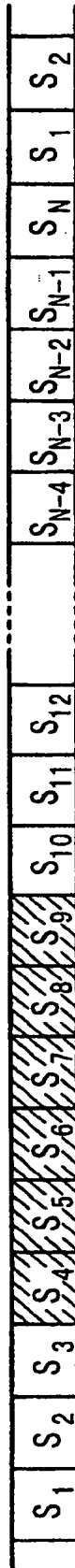


FIG. 11O
CORRECTED FRAME POSITION



FIG. 11P
CORRECTED FRAME POSITION



FIG. 12

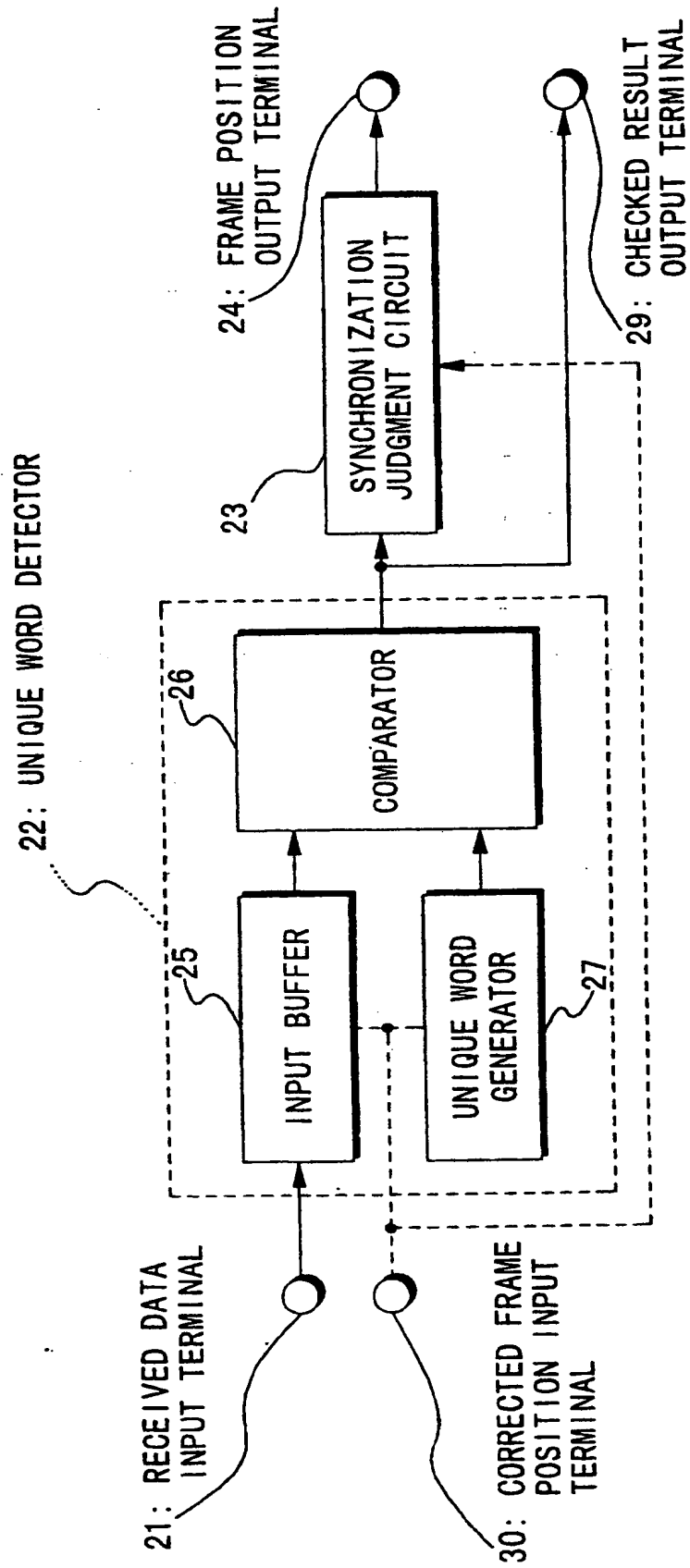


FIG. 13A
RECEIVED DATA SEQUENCE WITHOUT CODE ERROR

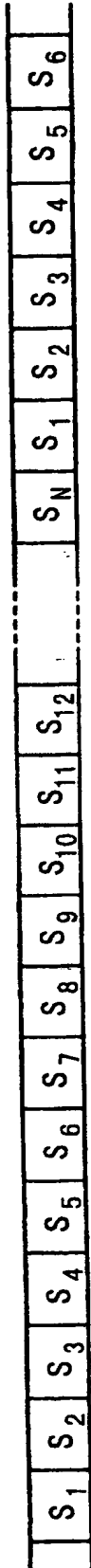


FIG. 13B
RECEIVED DATA SEQUENCE WITH CODE ERROR

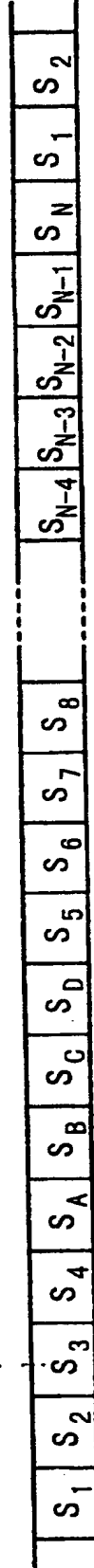


FIG. 13C
FIRST FRAME POSITION



FIG. 13D
REFERENCE UNIQUE WORD (FORWARD DIRECTION)

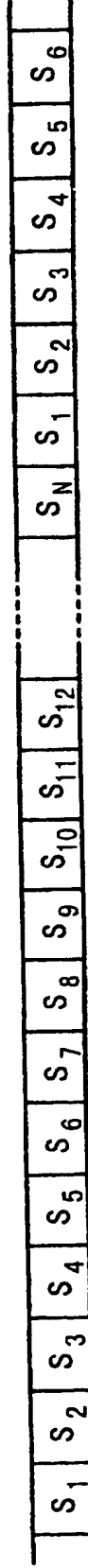


FIG. 13E
FIRST CHECKED RESULT



FIG. 13F
SECOND FRAME POSITION



FIG. 13G
REFERENCE UNIQUE WORD (BACKWARD DIRECTION)

S_{N-3}	S_{N-2}	S_{N-1}	S_N	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8		S_{N-4}	S_{N-3}	S_{N-2}	S_{N-1}	S_N	S_1	S_2
-----------	-----------	-----------	-------	-------	-------	-------	-------	-------	-------	-------	-------	--	-----------	-----------	-----------	-----------	-------	-------	-------

FIG. 13H
SECOND CHECKED RESULT

?	?	?	?	?	?	?	?	0	0	0	0		0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	---	---	---	---

DATA INSERTION OCCURRENCE POSITION
(FOR FOUR BITS)



FIG. 13I
FIRST CHECKED RESULT EXAMPLE (1)

0	0	0	0	1	0	0	1	1	0	1	0		?	?	?	?	?	?	?
---	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	---	---	---	---

FIG. 13J
SECOND CHECKED RESULT EXAMPLE (1)

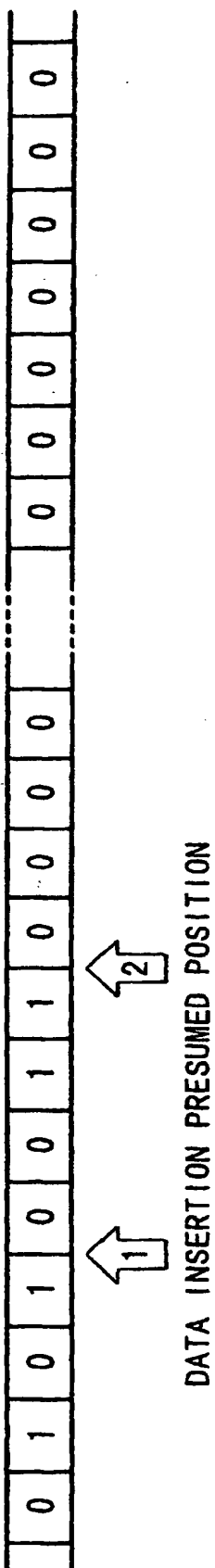


FIG. 13K
INSERTED DATA DELETION EXAMPLE (1)

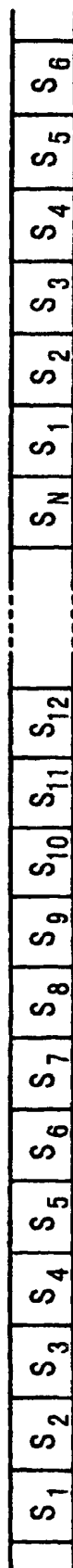


FIG. 14A
RECEIVED DATA SEQUENCE WITHOUT CODE ERROR

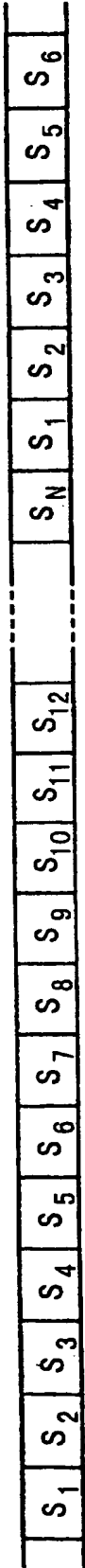


FIG. 14B
RECEIVED DATA SEQUENCE WITH CODE ERROR

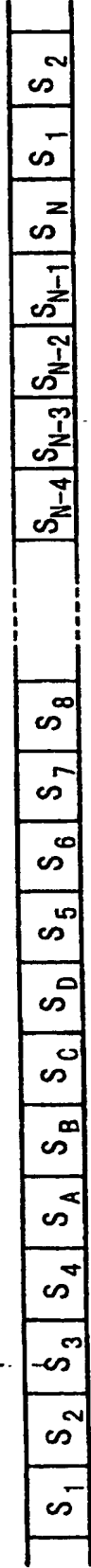


FIG. 14C
FIRST FRAME POSITION



FIG. 14D
REFERENCE UNIQUE WORD (FORWARD DIRECTION)

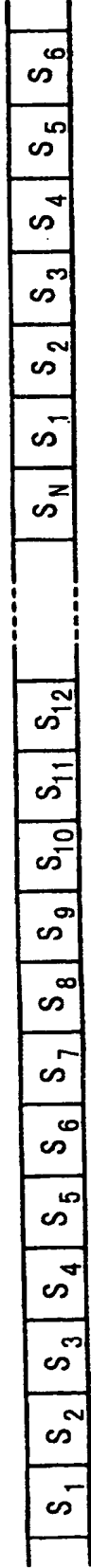


FIG. 14E
FIRST CHECKED RESULT



FIG. 14F
SECOND FRAME POSITION



FIG. 14G
REFERENCE UNIQUE WORD (BACKWARD DIRECTION)

S_{N-3}	S_{N-2}	S_{N-1}	S_N	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	-----	S_{N-4}	S_{N-3}	S_{N-2}	S_{N-1}	S_N	S_1	S_2
-----------	-----------	-----------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-----------	-----------	-----------	-----------	-------	-------	-------

FIG. 14H
SECOND CHECKED RESULT

?	?	?	?	?	?	?	?	0	0	0	0	-----	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	-------	---	---	---	---	---	---	---



INSERTION OCCURRENCE POSITION
(FOR FOUR BITS)

FIG. 14I
FIRST CHECKED RESULT EXAMPLE (2)

0	0	0	0	0	1	0	1	1	0	1	0	-----	?	?	?	?	?	?	?
---	---	---	---	---	---	---	---	---	---	---	---	-------	---	---	---	---	---	---	---

FIG. 14M
SECOND CHECKED RESULT EXAMPLE (2)



DATA INSERTION PRESUMED POSITION

FIG. 14N
DUMMY DATA INSERTION EXAMPLE (2)



FIG. 14O
CORRECTED FRAME POSITION



FIG. 14P
CORRECTED FRAME POSITION



FIG. 15A
RECEIVED DATA SEQUENCE WITHOUT CODE ERROR



FIG. 15B
RECEIVED DATA SEQUENCE WITH CODE ERROR



FIG. 15C
FIRST FRAME POSITION



FIG. 15D
REFERENCE UNIQUE WORD (FORWARD DIRECTION)



FIG. 15E
FIRST CHECKED RESULT



FIG. 15F
SECOND FRAME POSITION



FIG. 15G
REFERENCE UNIQUE WORD (BACKWARD DIRECTION)

S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁	S ₁₂	S ₁₃	S ₁₄	S ₁₅	S ₁₆	S _N	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆
----------------	----------------	----------------	----------------	----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------

FIG. 15H
SECOND CHECKED RESULT

?	?	?	?	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

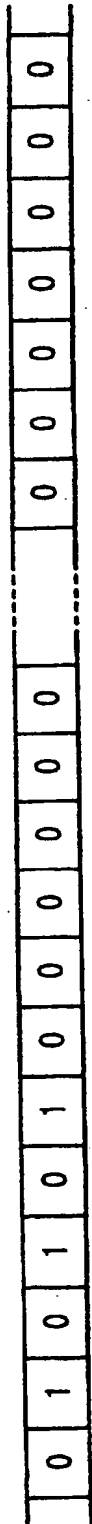


DATA LOSS OCCURRENCE POSITION
(FOR FOUR BITS)

FIG. 15I
FIRST CHECKED RESULT EXAMPLE

0	0	1	0	1	0	0	1	1	0	1	0	?	?	?	?	?	?	?
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

FIG. 15J
SECOND CHECKED RESULT EXAMPLE



DATA LOSS PRESUMED POSITION

FIG. 15K
DUMMY DATA INSERTION EXAMPLE (1)

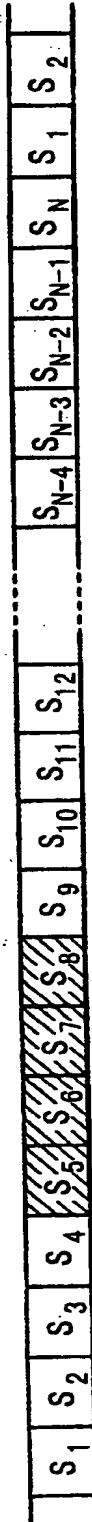


FIG. 15L
DUMMY DATA INSERTION EXAMPLE (2)



FIG. 15O
CORRECTED FRAME POSITION



FIG. 15P
CORRECTED FRAME POSITION



FIG. 16A
RECEIVED DATA SEQUENCE WITHOUT CODE ERROR

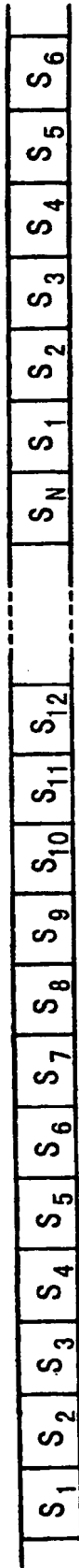


FIG. 16B
RECEIVED DATA SEQUENCE WITH CODE ERROR

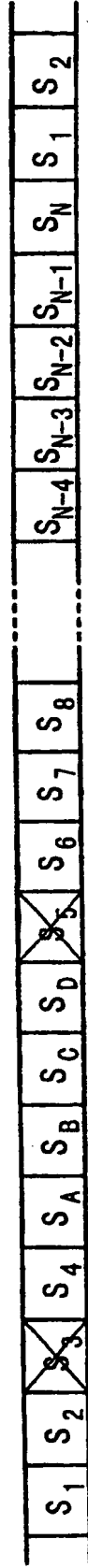


FIG. 16C
FIRST FRAME POSITION



FIG. 16D
REFERENCE UNIQUE WORD (FORWARD DIRECTION)



FIG. 16E
FIRST CHECKED RESULT



FIG. 16F
SECOND FRAME POSITION



FIG. 16G
REFERENCE UNIQUE WORD (BACKWARD DIRECTION)

S_{N-3}	S_{N-2}	S_{N-1}	S_N	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8		S_{N-4}	S_{N-3}	S_{N-2}	S_{N-1}	S_N	S_1	S_2
-----------	-----------	-----------	-------	-------	-------	-------	-------	-------	-------	-------	-------	--	-----------	-----------	-----------	-----------	-------	-------	-------

FIG. 16H
SECOND CHECKED RESULT

?	?	?	?	?	?	?	?	0	0	0	0		0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	---	---	---	---

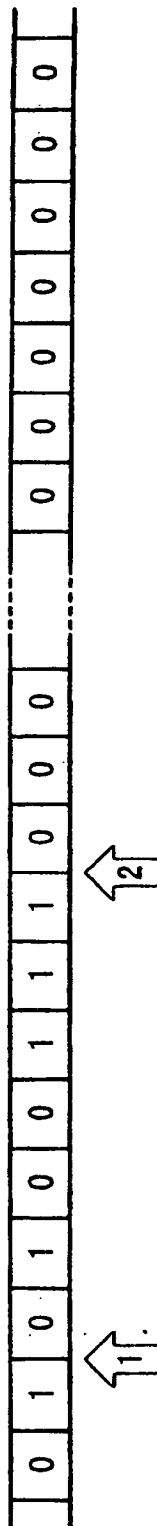


DATA INSERTION OCCURRENCE POSITION (FOR FOUR BITS)

FIG. 16I
FIRST CHECKED RESULT EXAMPLE (1)

0	0	1	0	1	0	0	1	1	0	1	0		?	?	?	?	?	?	?
---	---	---	---	---	---	---	---	---	---	---	---	--	---	---	---	---	---	---	---

FIG. 16J
SECOND CHECKED RESULT EXAMPLE (1)



DATA INSERTION PRESUMED POSITION

FIG. 16K
INSERTED DATA DELETION EXAMPLE (1)



FIG. 16L
INSERTED DATA DELETION EXAMPLE (2)

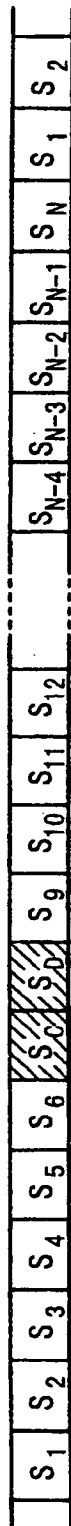


FIG. 16O
CORRECTED FRAME POSITION



FIG. 16P
CORRECTED FRAME POSITION



FIG. 17

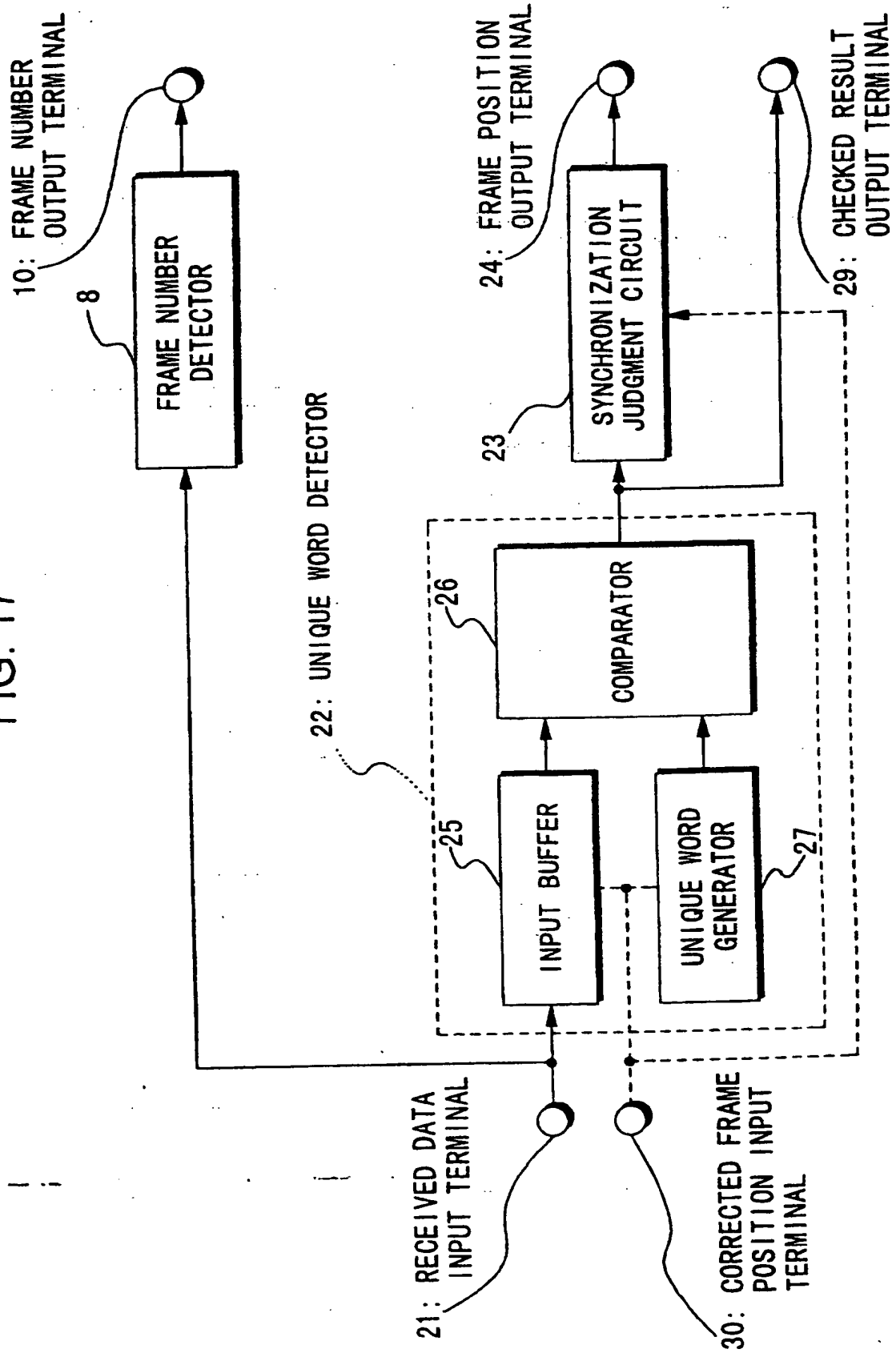


FIG. 18

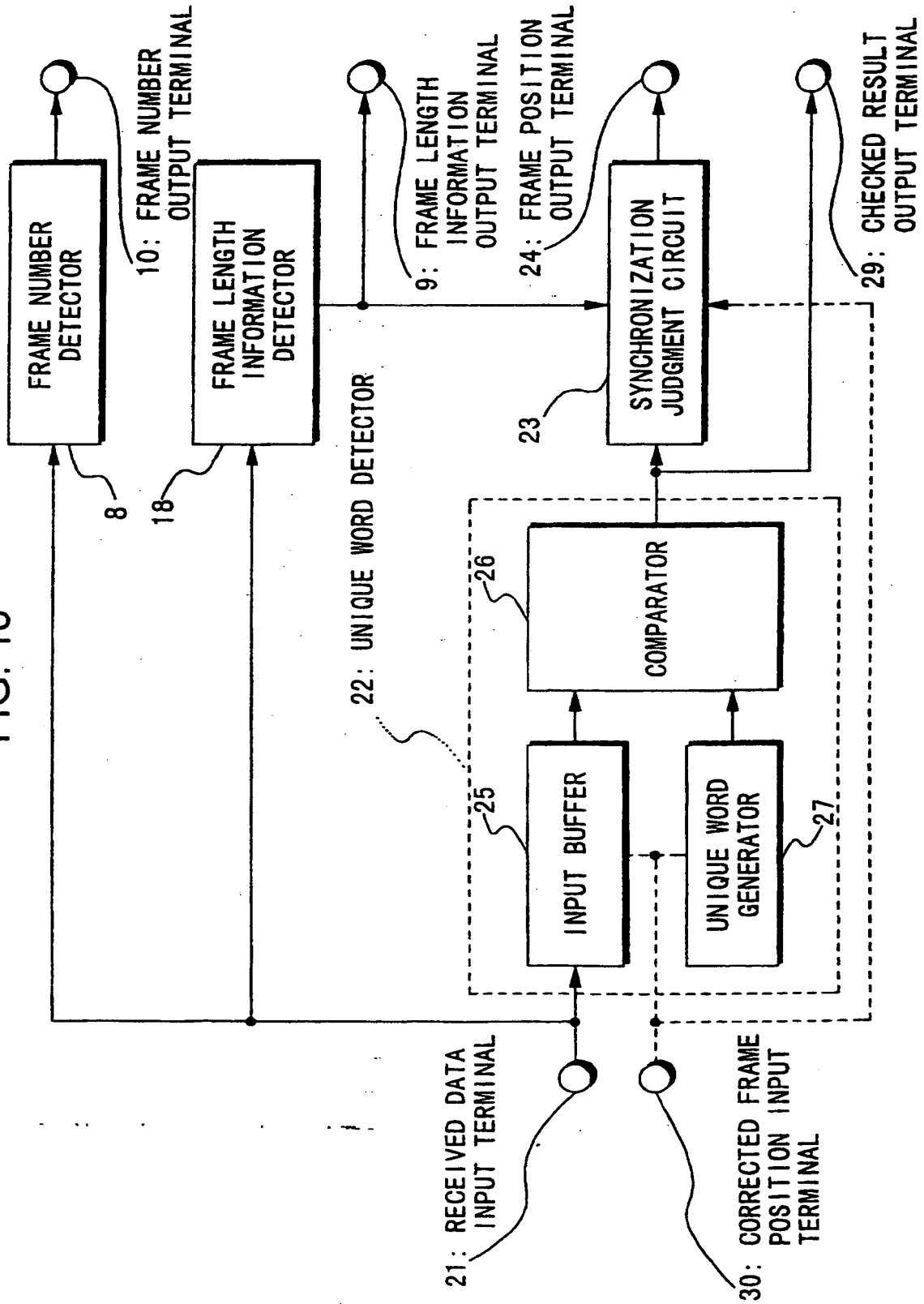


FIG. 19

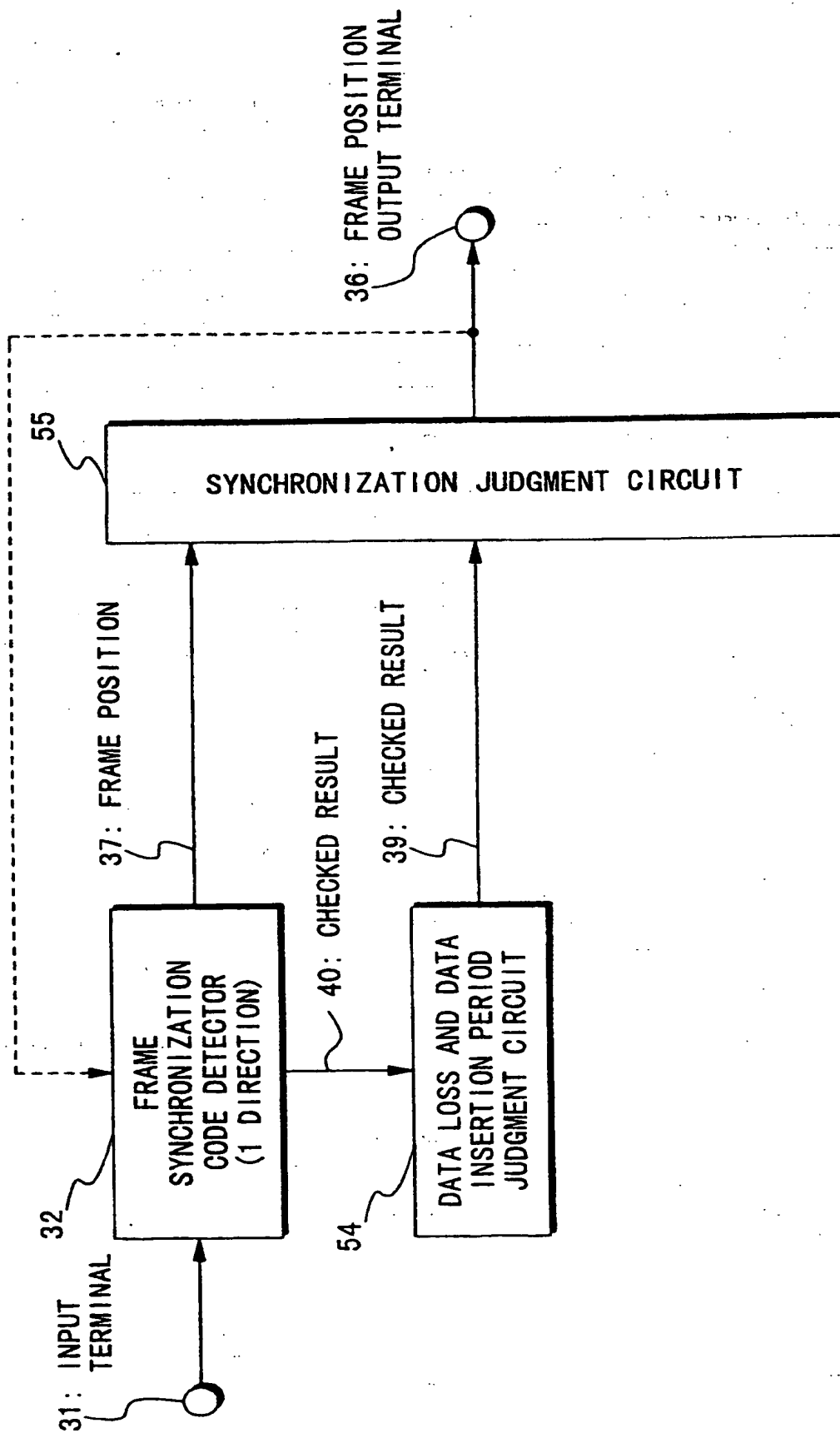


FIG. 20A
RECEIVED DATA SEQUENCE WITHOUT CODE ERROR

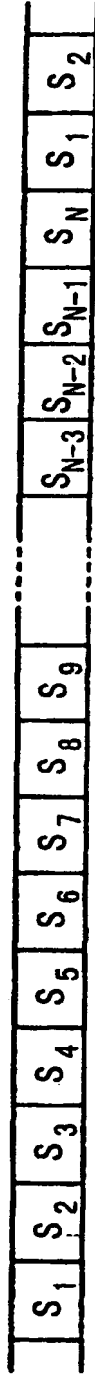


FIG. 20B
RECEIVED DATA SEQUENCE WITH CODE ERROR

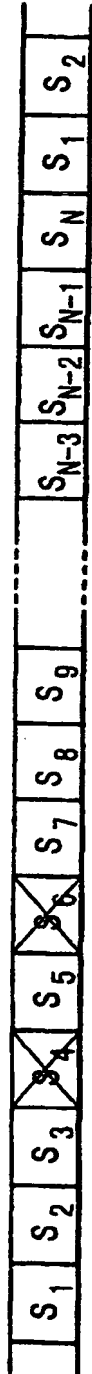


FIG. 20C
FRAME POSITION



FIG. 20D
REFERENCE UNIQUE WORD



FIG. 20E

CHECKED RESULT

[illegible]

FIG. 20F

ACCUMULATED RESULT OF EVALUATION VALUES

**JUDGING
THRESHOLD
VALUE**



FIG. 20G

JUDGMENT RESULT

GENERAL CODE ERROR

FIG. 21A
RECEIVED DATA SEQUENCE WITHOUT CODE ERROR



FIG. 21B
RECEIVED DATA SEQUENCE WITH CODE ERROR



FIG. 21C
FRAME POSITION



FIG. 21D
REFERENCE UNIQUE WORD

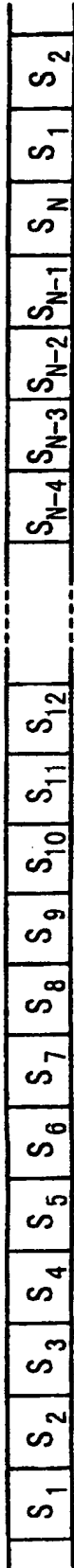


FIG. 21E
CHECKED RESULT

CHECKED RESULT



**DATA LOSS OCCURRENCE POSITION
(FOR FOUR BITS)**

FIG. 21F
EXAMPLE OF CHECKED RESULT

EXAMPLE OF CHECKED RESULT

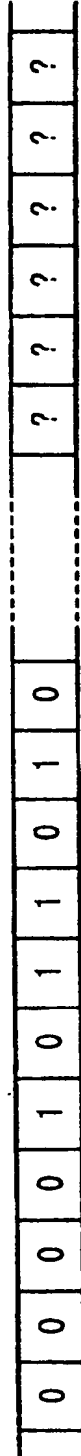


FIG. 21G
ACCUMULATED RESULT OF EVALUATION VALUES

ACCUMULATED RESULT OF EVALUATION VALUES

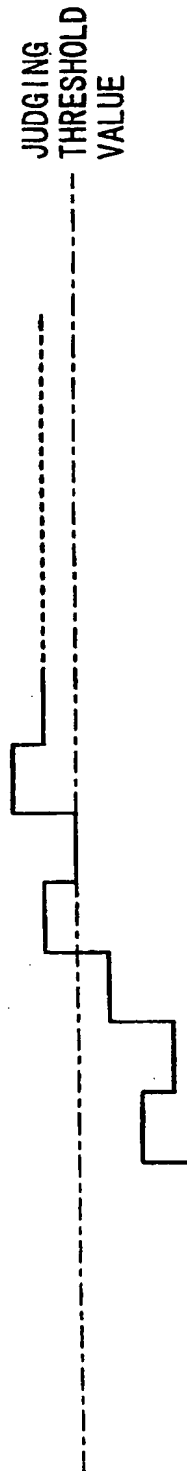


FIG. 21H
JUDGMENT RESULT

JUDGMENT RESULT

IN A CASE OF DATA LOSS

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP98/00557

A. CLASSIFICATION OF SUBJECT MATTER Int.Cl. ⁶ H04L7/08, H04J3/06		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) Int.Cl. ⁶ H04L7/08, H04J3/06		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Koho (Y1, Y2) 1926-1998 Toroku Jitsuyo Shinan Koho (U) 1994-1998 Kokai Jitsuyo Shinan Koho (U) 1971-1998 Jitsuyo Shinan Toroku Koho (Y2) 1996-1998		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	Sanae Hotani, Toshio Miki "Examination of Variable-Length Frame Synchronizing Method Suitable for MPEG-4 Audio (in Japanese)", Communication Society Convention of IEICE, Vol. 96 No. 481 RCS96-119, pages 35 to 42, 23. 01. 1997, Full text ; all drawings	1-5
A		6-11
Y	Toshiaki Watanabe, Yoshihiro Kikuchi, Ken Nakajo, Tsuyoshi Nagai Low Bit-Rate Moving Picture Coding Method adaptable to MPEG-4 (in Japanese)", Communication Society Convention of IEICE, Vol. 95 No. 581 IE95-145, pages 37 to 44, 14. 03. 1996, page 40, lines 6 to 25 ; Fig. 2	1-5
A		6-11
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search May 15, 1998 (15. 05. 98)		Date of mailing of the international search report May 26, 1998 (26. 05. 98)
Name and mailing address of the ISA/ Japanese Patent Office		Authorized officer
Facsimile No.		Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP98/00557

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 8-139714, A (Hitachi, Ltd., K.K. Hitachi Microsoft Systems), May 31, 1996 (31. 05. 96), Page 2, column 2, line 43 to page 3, column 3, line 18 ; page 4, column 5, line 49 to column 6, line 14 ; Fig. 1 (Family: none)	1-5
A		6-11

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

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